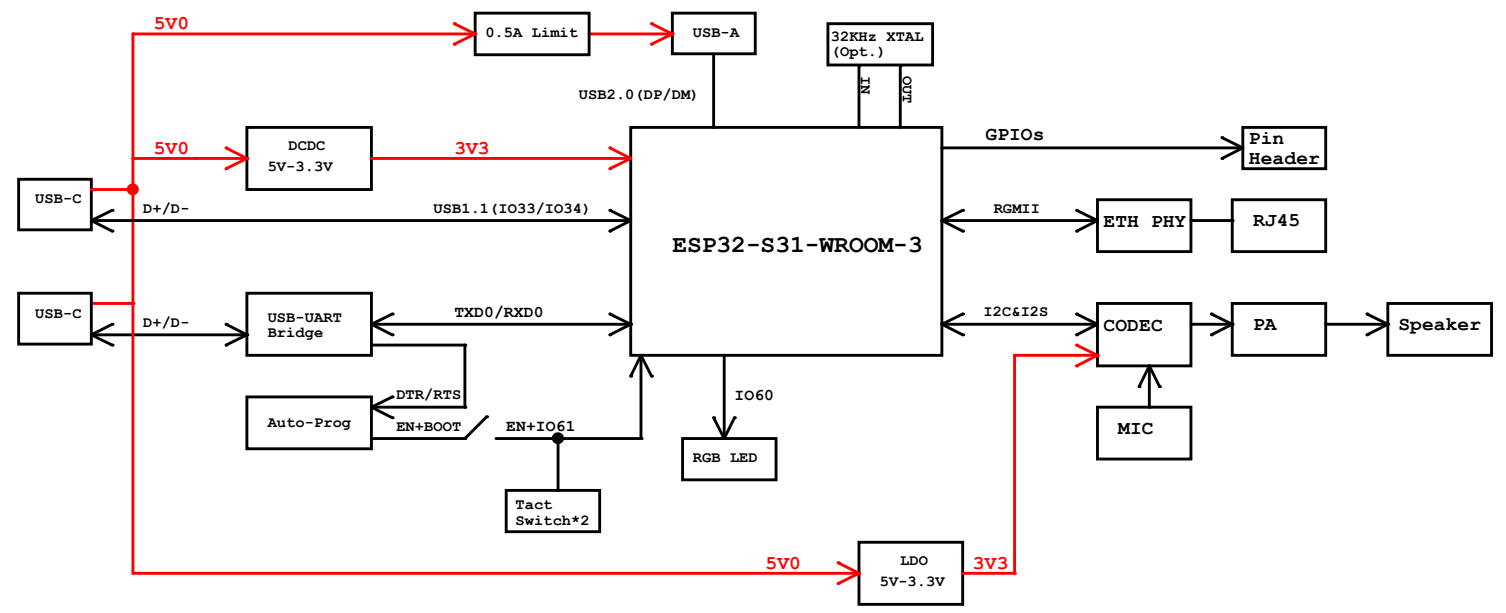
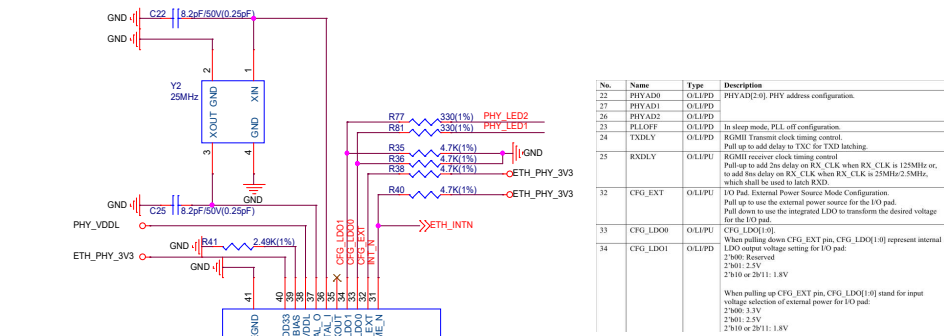
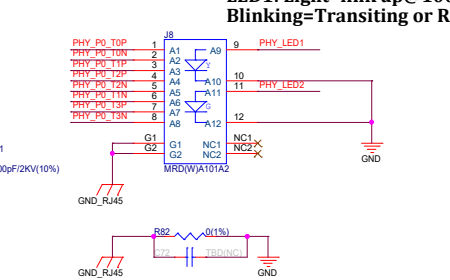
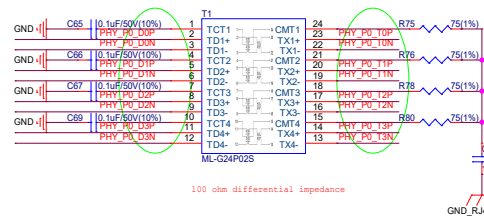
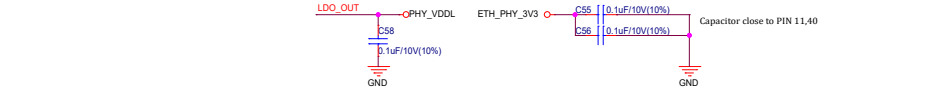
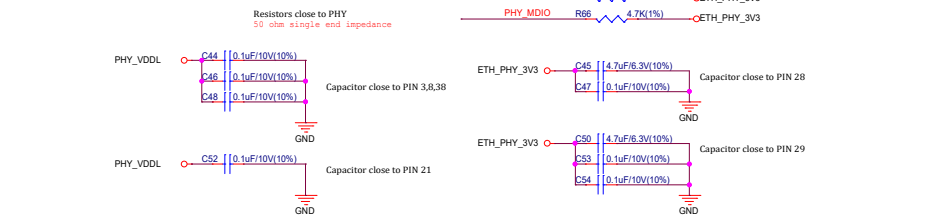
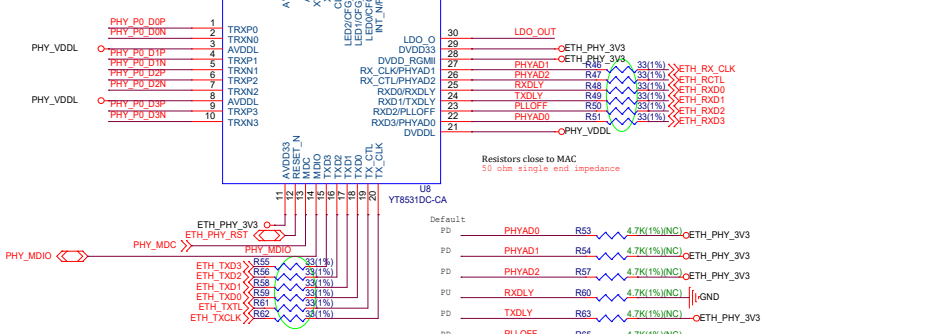


System Block:





No.	Name	Type	Description
22	PHYAD0	OL1PD	PHYAD[2:0], PHY address configuration.
27	PHYAD1	OL1PD	
26	PHYAD2	OL1PD	
24	TXDLY	OL1PD	In sleep mode, PLL self configuration.
25	RXDLY	OL1PU	RGMII transmit clock timing control. Pull up to add delay to TXC for TXD latching.
32	CFG_EXT	OL1PU	I/O pad. External Power Source Mode Configuration. Pull up to use the external power source for the I/O pad. Pull down to use the integrated LDO to transform the desired voltage for the I/O pad.
33	CFG_LDO0	OL1PU	CFG_LDO[1:0].
34	CFG_LDO1	OL1PD	When pulling down CFG_EXT pin, CFG_LDO[1:0] represent internal LDO output voltage setting for I/O pad. 2300: 2.3V 2340: 2.5V 2360 or 2011: 1.8V



Codec :

