



SMARTSENS

SmartSens™ **SC101IoT Datasheet**

V0.5

2022.06.16

■ Applications

- ◆ Dash Cameras
- ◆ Automotive Cameras (Front View, Backup and Full View)
- ◆ Smart Home Cameras
- ◆ Security Surveillance Cameras
- ◆ Mobile Device Camera
- ◆ Video Teleconferencing Equipment
- ◆ Industrial Endoscope Detector
- ◆ Detectoscope

■ Features

- ◆ Built-in programmable park line
- ◆ Dynamic park line
- ◆ Master/Slave SCCB control interface
- ◆ IR-CUT switching control
- ◆ Front light/back light mode
- ◆ LED supplementary lighting control
- ◆ 27MHz passive crystal input
- ◆ High sensitivity
- ◆ High signal to noise ratio
- ◆ Low power consumption
- ◆ 32x analog gain, 8x digital gain
- ◆ High speed DPC
- ◆ Horizontal/vertical mirror and flip
- ◆ Programmable I2C port register

■ Specifications

Parameters	Description
Resolution	1MP
Pixel array	1288H x 728V
Pixel size	2.9 μm x 2.9 μm
Optical format	1/4.2"
Maximum frame rate	1280H x 720V@30fps 8-bit
Output interface	25fps/30fps 8-bit DVP
Output format	RAW RGB/YUV422
CRA	15°
Sensitivity	7280 mV/lux • s
Dynamic range	83 dB
SNR	41 dB
Operation temperature range	-30°C ~ +85°C
Best IQ temperature	-20°C ~ +60°C
Power supply	AVDD = 2.8V $\pm$ 0.1V, DOVDD = 2.8V $\pm$ 0.1V Note: For DVDD, internal power supply is recommended by default; if you want to use external power supply scheme, please contact FAE.
Package	CSP, 4.318 mm x 3.230 mm, 35-pin
ESD rank	■ HBM: Classification 2 ■ CDM: Classification C3

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1. System Description

1.1. General Description

SC101IoT is an advanced digital CMOS image sensor for surveillance cameras, supporting 25fps/30fps coaxial analog high definition and 8bit RAW RGB/YUV422 DVP output. It outputs raw images with an effective pixel array of 1288H × 728V and supports multiple hardware control modes such as windowing, horizontal or vertical mirroring, and so on.

It can be configured via the standard I2C interface. It has built-in I2C master for initial configuration through external E2PROM.

1.2. System Framework

Figure 1-1 shows the block diagram of SC101IoT. SC101IoT supports DVP and HD-Analog interfaces. Figure 1-2 shows typical configuration diagram.

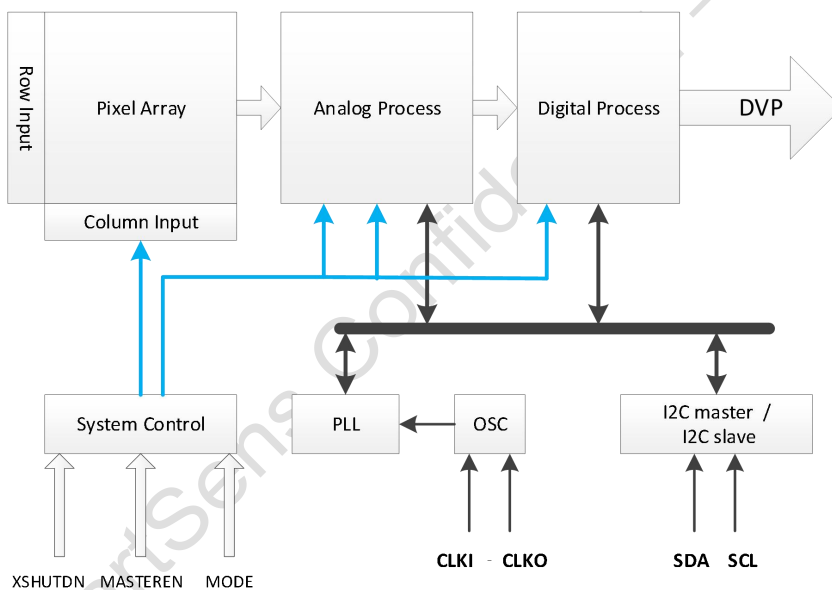


Figure 1-1 Block diagram

SC101IoT supports DVP, the typical circuit as follows:

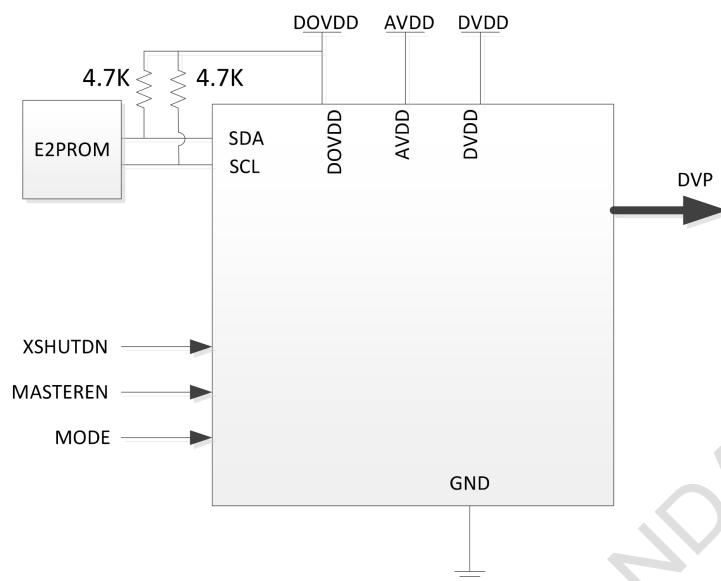


Figure 1-2 Typical configuration diagram

1.3. Pin Description

The table below lists the pin information and related description of SC101IoT.

Table 1-1 Pin description

No.	Pin No.	Pin Name	Pin Type	Description
1	A1	AVDD	Power	Analog Power Supply
2	A2	NC	-	-
3	A3	LREF	Output	DVP Row Synchronization Signal When Output
4	A4	SDA	Input / Output	I2C Data Line (open drain)
5	A5	DGND	GND	Digital Ground
6	A6	XSHUTDN	Input	Reset Signal Input (internal pull-up, active low)
7	A7	DGND	GND	Digital Ground
8	B1	AGND	GND	Analog Ground
9	B2	XCLKI	Input	Input Clock
10	B3	FSYNC	Output	DVP Frame Synchronization Signal
11	B4	SCL	Input / Output	Master/Slave I2C Clock Line (open drain)
12	B5	DOGND	GND	I/O Ground
13	B6	DGND	GND	Digital Ground
14	B7	DVDD	Power	For DVDD, internal power supply is recommended by default; if you want to use external power supply scheme, please contact FAE.
15	C1	DVDD	Power	For DVDD, internal power supply is recommended by default; if you want to use external power supply scheme, please contact FAE.
16	C2	DVDD	Power	For DVDD, internal power supply is recommended by default; if you want to use external power supply scheme, please contact FAE.
17	C3	DOGND	GND	I/O Ground
18	C4	PCLK	Output	DVP Clock
19	C5	DOVDD	Power	I/O Power Supply
20	C6	DVDD	Power	For DVDD, internal power supply is recommended by default; if you want to use external power supply scheme, please contact FAE.
21	C7	AGND	GND	Analog Ground
22	D1	D<0>	Output	DVP Output Bit[0]
23	D2	D<2>	Output	DVP Output Bit[2]
24	D3	D<5>	Output	DVP Output Bit[5]
25	D4	D<6>	Output	DVP Output Bit[6]
26	D5	NC	-	-
27	D6	AVDD	Power	Analog Power Supply
28	D7	VREF1	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)
29	E1	D<1>	Output	DVP Output Bit[1]
30	E2	D<3>	Output	DVP Output Bit[3]
31	E3	D<4>	Output	DVP Output Bit[4]
32	E4	D<7>	Output	DVP Output Bit[7]

No.	Pin No.	Pin Name	Pin Type	Description
33	E5	AVDD	Power	Analog Power Supply
34	E6	NC	-	-
35	E7	VREFN	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)

Top View

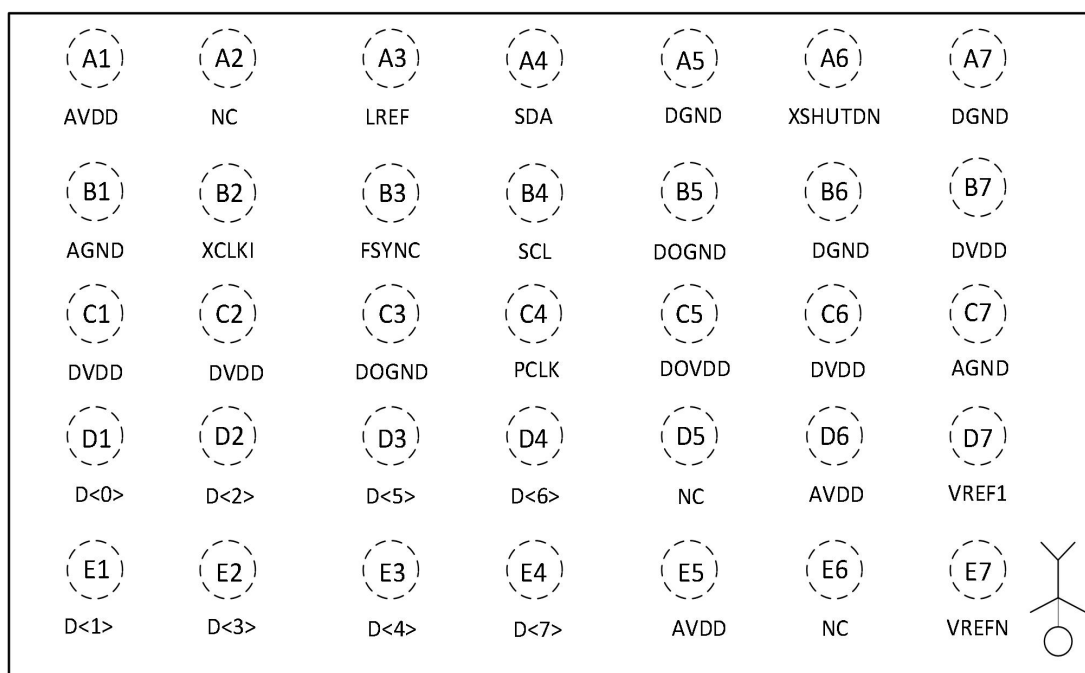


Figure 1-3 Top view of SC101IoT package pin assignment

1.4. Chip Initialization

1.4.1. Power-on Timing

During power-on, the specific power-on timing requirements shown below.

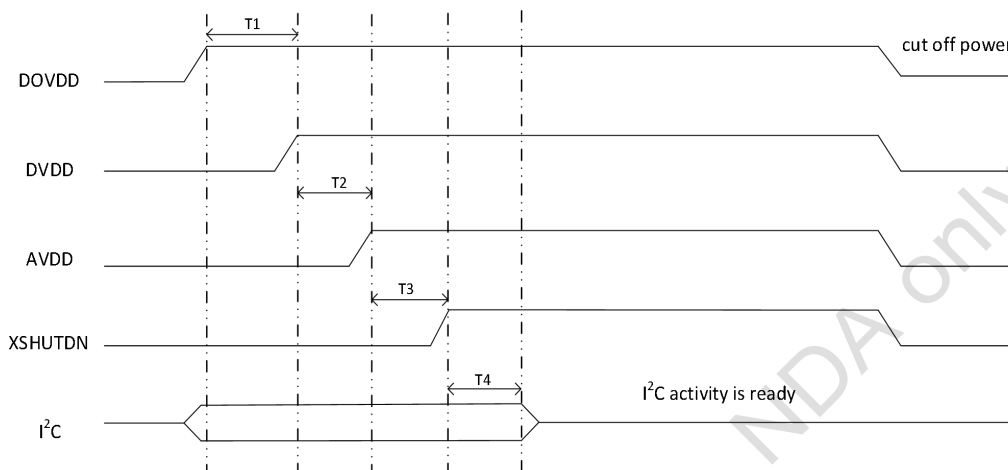


Figure 1-4 Power-on timing

Note: T1≥0ms, T2≥0ms, T3≥0ms, T4≥12ms.

1.4.2. I2C Master/Slave Mode

SC101IoT controls I2C master/slave mode selection via the MASTEREN pin.

1. Pull the MASTEREN pin high, I2C enters master mode, sensor reads the initialization configuration of E2PROM, and releases I2C bus after initialization to enter slave mode.
2. Pull the MASTEREN pin low, I2C enters slave mode.

1.4.3. I2C Paging Mode

The SC101IoT register uses paging mode. The 16-bit I2C address described in the register table is divided into the high 8-bit address and the low 8-bit address. The high 8-bit address is fixed as the register value and written to the address 0xf0. The corresponding register value is written to the low 8-bit address. Examples are as follows:

Write 0x3103, 0x01

The actual I2C writing sequence should be:

0xf0, 0x31

0x03, 0x01

1.4.4. Reset Mode

During reset, this chip stops outputting data, works in a low power status, and resets its registers. This chip offers two approaches to reset:

1. Hard reset: pull the XSHUTDOWN pin low, registers access through I²C is not supported.
2. Soft reset: write 1 to register 16'h3103[0], reset mode lasts for 150 ns.

Table 1-2 Soft reset control register

Function	Address	Default Value	Description
Paging register	8'hf0	8'h31	Paging
Soft reset	8'h03	8'h00	Bit[0]: soft reset 0: disable 1: enable

1.5. Configuration Interface

Registers of this chip can be read and written via the standard I²C bus. The I²C bus device address of the I²C interface is 0xd0. The first line of Figure 1-5 shows a standard I²C communication protocol for 7-bit slave address, 8-bit sub address and 8-bit data. The slave address is the I²C bus device address. The second line of Figure 1-5 shows a write operation. The third line of Figure 1-5 shows a read operation. Figure 1-6 shows the I²C timing diagram.

Standard I²C communication protocol

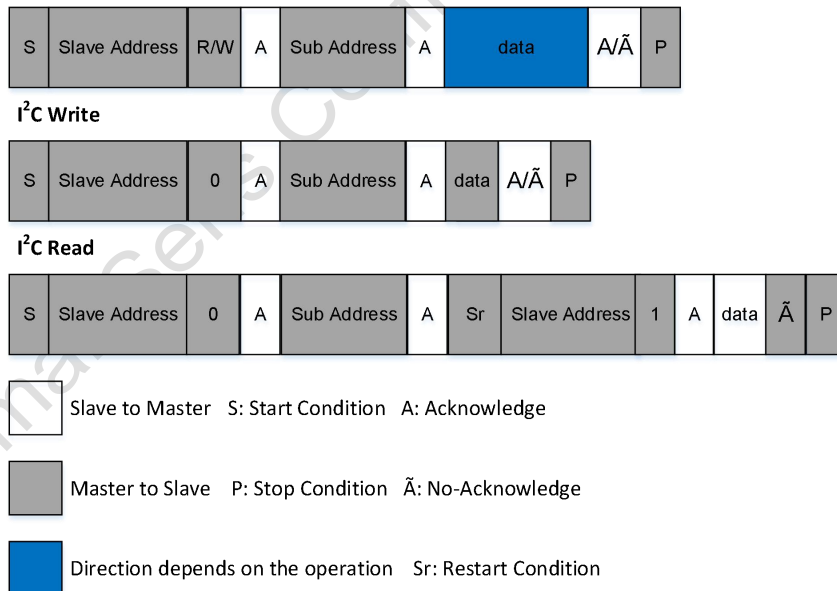


Figure 1-5 I²C standard protocol

I²C interface timing

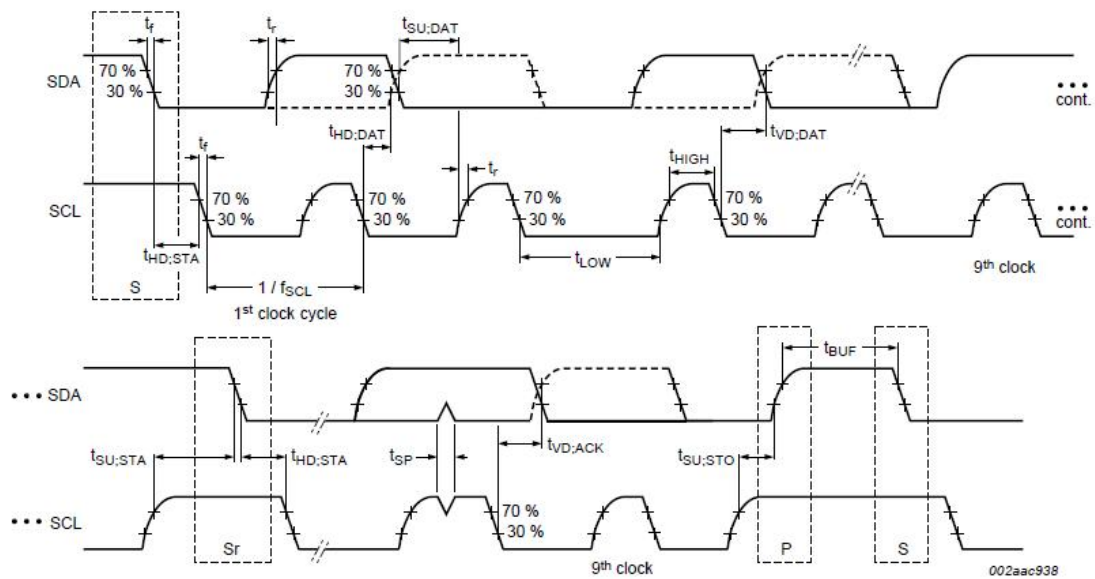


Figure 1-6 I²C interface timing

Table 1-3 I²C interface timing parameter

Symbol	Parameter	Standard-mode		Fast-mode		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;STA}$	hold time (repeated) START condition	4.0	-	0.6	-	μs
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	μs
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	μs
$t_{SU;STA}$	set-up time for a repeated START condition	4.7	-	0.6	-	μs
$t_{HD;DAT}$	data hold time	0	-	0	-	μs
$t_{SU;DAT}$	data set-up time	250	-	100	-	ns
t_r	rise time of both SDA and SCL signals	-	1000	20	300	ns
t_f	fall time of both SDA and SCL signals	-	300	20	300	ns
$t_{SU;STO}$	set-up time for STOP condition	4.0	-	0.6	-	μs
t_{BUF}	bus free time between a STOP and START condition	4.7	-	1.3	-	μs
$t_{VD;DAT}$	data valid time	-	3.45	-	0.9	μs
$t_{VD;ACK}$	data valid acknowledge time	-	3.45	-	0.9	μs
t_{SP}	pulse width of spikes that must be suppressed by the input filter	-	-	0	50	ns

Note: The beginning of a rising edge and the end of a falling edge are at 30% of the amplitude of the signal. The end of a rising edge and the beginning of a falling edge are at 70% of the amplitude of the signal.

1.6. Sensor ID

Table 1-4 Sensor ID control register

Function	Register	Default Value	Description
SENSOR ID high	8'hf7	8'hda	SENSOR ID[15:8]
SENSOR ID low	8'hf8	8'h4a	SENSOR ID[7:0]

1.7. Data Interface

There is a data interfaces in this chip: the Digital Video Port (DVP).

1.7.1. Digital Video Port (DVP)

This chip provides a Digital Video Port (DVP) that outputs 8-bit parallel data. Data frame synchronization signal is outputted from the FSYNC pin, line synchronization signal is outputted from the LREF pin, and the data clock signal is outputted from the PCLK pin. The figure below shows the DVP timing diagram.



Figure 1-7 DVP timing diagram

Table 1-5 DVP timing control register

Function	Address	Default Value	Description
DVP output	16'h0176	8'h20	Bit[7]: data output enable 1: enable, 0: disable
			Bit[5]: 1: data_out[1:0] is IR drive; 0: data output
			Bit[4]: 1: IR drive is [0:1]; 0: IR drive is [1:0]
DVP signal polarity	16'h017a	8'h06	Bit[5]: 0: Fsync is high active; 1: Fsync is low active
			Bit[4]: 0: LREF is high active; 1: LREF is low active
	16'h0177	8'h80	Bit[3]: PCLK enable 0: disable (high output); 1: enable (clock output) Bit[2]: 0: PCLK normal output; 1: PCLK invert
PAD driving capability	16'h3641	8'h00	Bit[1:0]: adjust PAD driver capability
Pclk delay	16'h3640	8'h00	Bit[1:0]: step 2ns.

8bit RAW RGB /YUV422 output is supported in DVP mode.

Table 1-6 Image mode register

Function	Address	Default Value	Description
Image mode	16'h0179	8'h00	Bit[1:0]: when YCbCr422 enable 2'b00: YCbYCr; 2'b01: YCrYCb; 2'b10: CbYCrY; 2'b11: CrYCbY;
	16'h0177	8'h80	Bit[0]: 1'b0: YCbCr422 1'b1: bayer raw_data(0x00e0h=8'h40)

1.8. Phase Locked Loop (PLL)

The input clock frequency of the PLL module ranges from 6 MHz to 40 MHz, while the VCO output frequency (F_{VCO}) ranges from 400 MHz to 1200 MHz. The PLL block diagram is shown in Figure 1-8.

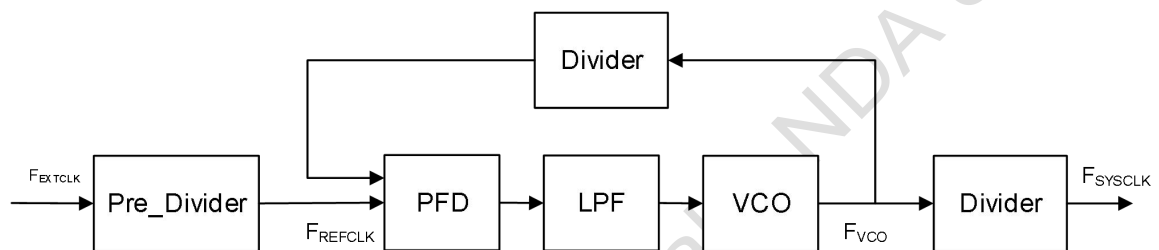


Figure 1-8 PLL control diagram

1.9. Video Output Mode

1.9.1. Read Order

Below figure shows the location of the first read pixel as well as the entire array structure. This figure shows the top view when the A1 pin is placed in the upper left corner. The figure below shows the first pixel data color format.

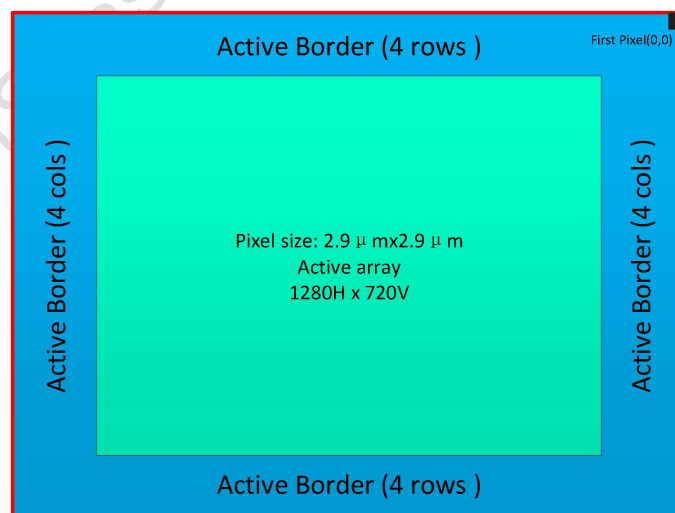


Figure 1-9 Pixel array 1

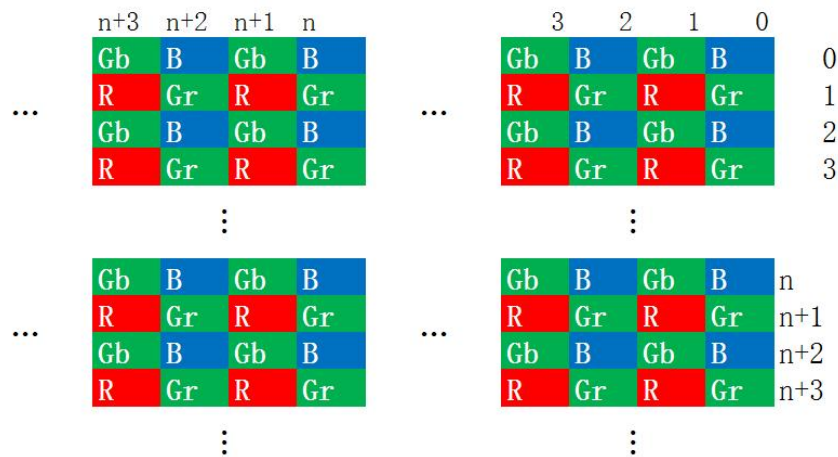


Figure 1-10 Pixel array 2

This chip supports the mirror mode and the flip mode. The mirror mode reverses the sensor data read out order, and the flip mode vertically reverses the sensor readout order, as shown in Figure 1-11.



Figure 1-11 Mirror/flip example

Table 1-7 Mirror and flip control registers

Function	Address	Default Value	Description
Mirror	16'h3221	8'h00	Bit[2:1]: mirror ctrl
			2'b00~mirror off
			2'b11~mirror on
Flip	16'h3221	8'h00	Bit[6:5]: flip ctrl
			2'b00~flip off
			2'b11~flip on

1.9.2. Output Window

Table 1-8 Output window registers

Function	Address	Default Value	Description
Column start	{0x0172[3:0], 0x0170}	12'h002	Output column start
Column end	{0x0172[7:4], 0x0171}	12'h502	Output column end
Row start	{0x0175[3:0], 0x0173}	12'h002	Output row start
Row end	{0x0175[7:4], 0x0174}	12'h2d2	Output row end

1.10. Test Mode

For the ease of testing, this chip provides color bars mode as shown below.

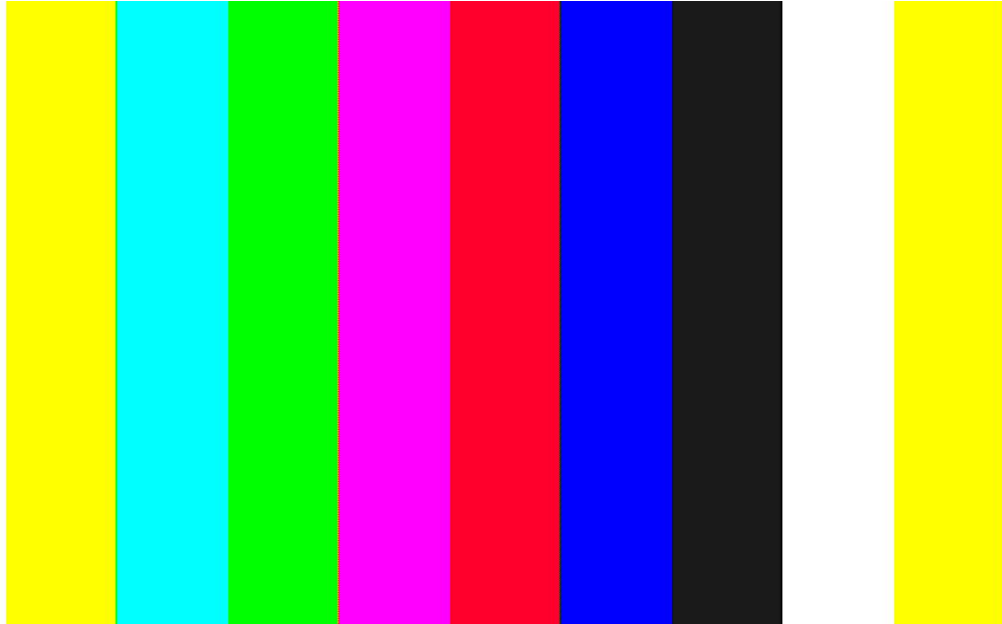


Figure 1-12 Test mode

Table 1-9 Test mode control registers

Function	Address	Register value	Description
Test mode	16'h0100	8'h00	Bit[7]: 1: test pattern enable 0: bypass test pattern
			Bit[6]: 1: shade test pattern, 0: disable
			Bit[5]: Reserved
			Bit[4]: manual write R/G/B
			Bit[3]: 0: vertical pattern 1: horizontal pattern
			Bit[2:0]: select the color
	16'h0101	8'h80	define R value
	16'h0102	8'h80	define G value
	16'h0103	8'h80	define B value

1.11. Gamma

The image signal needs to be compensated for the non-linear attenuation of the image brightness by the display device, i.e. gamma correction. The gamma control register in SC101IoT is shown in the following table.

Table 1- 10 Gamma control register

Function	Address	Default value	Description
GAMMA switch	16'h00f5[1]	1'b0	GAMMA enable 0~enable; 1~disable
Gamma endpoint 1	16'h0041	8'h13	Gamma coefficient1
Gamma endpoint 2	16'h0042	8'h24	Gamma coefficient2
Gamma endpoint 3	16'h0043	8'h41	Gamma coefficient3
Gamma endpoint 4	16'h0044	8'h6b	Gamma coefficient4
Gamma endpoint 5	16'h0045	8'h8a	Gamma coefficient5
Gamma endpoint 6	16'h0046	8'ha0	Gamma coefficient6
Gamma endpoint 7	16'h0047	8'hb2	Gamma coefficient7
Gamma endpoint 8	16'h0048	8'hc0	Gamma coefficient8
Gamma endpoint 9	16'h0049	8'hcc	Gamma coefficient9
Gamma endpoint 10	16'h004a	8'hd5	Gamma coefficient10
Gamma endpoint 11	16'h004b	8'hdd	Gamma coefficient11
Gamma endpoint 12	16'h004c	8'he4	Gamma coefficient12
Gamma endpoint 13	16'h004d	8'hf0	Gamma coefficient13
Gamma endpoint 14	16'h004e	8'hf8	Gamma coefficient14
Gamma endpoint 15	16'h004f	8'hff	Gamma coefficient15

1.12. Defect Pixel Correction (DPC)

SC101IoT supports real-time defect pixel identification and correction. The recognition and correction of 1 pixel, 1*2 same color defect pixel clusters and 3 or 4 same color defect pixel clusters can be realized. The defect pixel of SC101IoT is determined based on the principle that the current pixel value is larger (or smaller) than the pixel values of the same color around, and the difference value is greater than the set threshold value. SC101IoT divides defect pixel into white pixel and black pixel according to the principle. The specific control registers are shown in the following table.

Table 1- 11 Defect pixel control register

Function	Address	Default value	Description
Single defect pixel cluster correction	16'h00e0[2]	1'b1	Single defect pixel cancellation enable 1~enable; 0~disable
White defect pixel cluster correction	16'h00e0[3]	1'b1	Bright couplet defect pixels cancellation enable 1~enable; 0~disable
Black defect pixel cluster correction	16'h00e0[5]	1'b0	Dark couplet defect pixels cancellation enable 1~enable; 0~disable
Big defect pixel cluster correction	116'h00e7[7]	1'b0	Big defect cluster pixels cancellation enable 1~enable; 0~disable

1.13. Noise Correction

SC101IoT realizes noise correction through lpf1~lpf3, and the intensity of noise correction is adaptively changed through gain. The specific control registers are shown in the following table.

Table 1- 12 Noise correction control register

Function	Description	Address	Default value	Description
LPF1	Switch	16'h00e0[0]	1'b1	lpf1 enable 1~enable; 0~disable
	Reference intensity	16h00d5[3:0]	4'h4	The base strength of lpf 1
	Intensity change rate	16h00d6[3:0]	4'h2	The rate of change of lpf1 strength
LPF2	Switch	16'h00e0[0]	1'b1	lpf2 enable 1~enable; 0~disable
	Reference intensity	16h00d5[7:4]	4'h2	The base strength of lpf 2
	Intensity change rate	16h00d6[7:4]	4'h2	The rate of change of lpf2 strength
LPF3	Switch	16'h00e0[0]	1'b1	lpf3 enable 1~enable; 0~disable
	Reference intensity	16h00d3[7:4]	4'h0	The base strength of lpf 3
	Intensity change rate	16h00d8[7:4]	4'h2	The rate of change of lpf3 strength

1.14. Edge Enhancement

SC101IoT supports edge enhancement function, which can realize separate control of positive and negative edges of input image. Edge enhancement can realize adaptive control according to gain change. The specific control registers are shown in the following table.

Table 1- 13 Edge enhancement control register

Function	Address	Default value	Description
Edge enhancement switch	16'h00e0[1]	1'b1	Edge enhancement enable 1~enable; 0~disable
Negative edge enhancement reference	16h00d0[3:0]	4'h6	Edge enhancement strength control for negative edge
Positive edge enhancement reference	16h00d0[7:4]	4'h6	Edge enhancement strength control for positive edge
Negative edge enhancement limit coefficient	16'h00d2[3:0]	4'h6	Lower limit of edge enhancement (0~1.875)
Positive edge enhancement limit coefficient	16h00d2[7:4]	4'h6	Upper limit of edge enhancement (0~1.875)

1.15. AEC/AGC

AEC/AGC are all adjusted based on brightness. AEC adjusts exposure time and AGC adjusts gain value to finally make the image brightness fall within the set brightness threshold range. SC101IoT supports manual exposure and automatic exposure.

1.15.1. Manual Exposure Setting

When 16'h0070[0] is set to 0, the integration time manual configuration mode is entered.

When 16'h0070[1] is set to 0, the manual configuration mode of global gain and digital gain is entered. When 16'h0072[7] is set to 0, the global gain and digital gain are combined for configuration, and SC101IoT automatically calculates the corresponding global gain and digital gain. When 16'h0072[7] is set to 1, the global gain and the digital gain are configured separately. The specific control registers are shown in the following table.

Table 1- 14 Manual exposure control register

Function	Address	Default value	Description
AEC control switch	16'h0070[0]	1'b1	AEC control 1~auto; 0~manual
AGC control switch	16'h0070[1]	1'b1	AGC control 1~auto; 0~manual
Global gain, digital gain control modes	16'h0072[7]	1'b0	Global gain and digital gain control 1~independent; 0~non independent
Integration time	{16'h008d, 16'h008e}	16'h136	Integration time
Global gain	{16'h008b[3:0], 16'h008c}	12'h032	Global gain
Digital gain	16'h009e	8'h50	Digital gain

1.15.2. Automatic Exposure Setting

When 16'h0070[1:0] is set to 2'b11, the automatic exposure mode is entered. SC101IoT sets the corresponding integration time, global gain and digital gain according to the brightness characteristics of the current image. SC101IoT divides the image into 16 windows to evaluate brightness characteristics. In addition, the front light and back light modes can be set, or the automatic conversion modes of front light and back light can be set. The window settings are shown in the following figure.

Win1	Win2	Win3	Win4
Win5	Win6	Win7	Win8
Win9	Win10	Win11	Win12
Win13	Win14	Win15	Win16

Figure 1- 13 AE window settings

The register control of automatic exposure is shown in the following table.

Table 1- 15 Automatic exposure control register

Function	Address	Default value	Description
AEC control switch	16'h0070[0]	1'b1	AEC control 1~auto; 0~manual
AGC control switch	16'h0070[1]	1'b1	AGC control 1~auto; 0~manual
Automatic exposure target value	16'h0072[6:0]	7'h40	*2, AE target
Front light mode switch	16'h0070[6]	1'b1	Front light control enable 1~enable; 0~disable
Back light mode switch	16'h0086[7]	1'b0	Back light Control enable 1~enable; 0~disable
Window weight setting 1	16'h0068	8'h00	[7:6]: Weight1 of window4 [5:4]: Weight1 of window3 [3:2]: Weight1 of window2 [1:0]: Weight 1of window1
Window weight setting 2	16'h0069	8'hff	[7:6]: Weight1 of window8 [5:4]: Weight1 of window7 [3:2]: Weight1 of window6 [1:0]: Weight1 of window5
Window weight setting 3	16'h006a	8'hff	[7:6]: Weight1 of window12 [5:4]: Weight1 of window11 [3:2]: Weight1 of window10 [1:0]: Weight1 of window9
Window weight setting 4	16'h006b	8'hff	[7:6]: Weight1 of window16 [5:4]: Weight1 of window15 [3:2]: Weight1 of window14 [1:0]: Weight1 of window13

1.16. AWB

Due to different color temperatures, white objects show different colors. For example, under low color temperature (light A), white objects are red, and under high color temperature (D65), white objects are blue. In order to ensure the visual authenticity, white objects with different color temperatures need to be finally presented as white, which requires corresponding adjustment of blue gain and red gain, that is, white balance. SC101IoT supports automatic white balance and manual white balance. In automatic white balance, sensor automatically calculates blue and red gains according to image features; in manual white balance, the blue and red gains can be set directly. The specific control registers are shown in the following table.

Table 1- 16 AWB control registers

Function	Address	Default value	Description
Auto white balance switch	16'h00b0[0]	1'b1	AWB enable 1~enable; 0~disable

Function	Address	Default value	Description
Blue gain	16h00c8	8'h90	Blue gain
Red gain	16h00c9	8'h34	Red gain

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1.17. Color Correction

Due to the problem of optical crosstalk between pixels, there are differences between colors generated by image sensors and colors in nature. In order to make up for such differences, color correction is needed in signal processing. SC101IoT uses a color correction matrix of 3*3 to correct the color of the input image.

$$\begin{bmatrix} R' \\ G' \\ B' \end{bmatrix} = \begin{bmatrix} CMatrix11 & CMatrix12 & CMatrix13 \\ CMatrix21 & CMatrix22 & CMatrix23 \\ CMatrix31 & CMatrix32 & CMatrix33 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

Here, $\begin{bmatrix} R \\ G \\ B \end{bmatrix}$ is the color value of the uncorrected pixel, $\begin{bmatrix} R' \\ G' \\ B' \end{bmatrix}$ is the color value of the corrected pixel.

The specific control registers are shown in the following table.

Table 1- 17 Color correction control register

Function	Address	Default value	Description
Color correction switch	16'h00f5[2]	1'b0	Color correction control enable 0~enable; 1~disable
Cmatrix11	16'h0120	8'h10	color matrix coefficient 1
Cmatrix12	16'h0121	8'h88	color matrix coefficient 2
Cmatrix13	16'h0122	8'h88	color matrix coefficient 3
Cmatrix21	16'h0123	8'h8a	color matrix coefficient 4
Cmatrix22	16'h0124	8'h15	color matrix coefficient 5
Cmatrix23	16'h0125	8'h8b	color matrix coefficient 6
Cmatrix31	16'h0126	8'h08	color matrix coefficient 7
Cmatrix32	16'h0127	8'hb0	color matrix coefficient 8
Cmatrix33	16'h0128	8'h28	color matrix coefficient 9

1.18. Saturation

SC101IoT can control the saturation of blue and red respectively. The specific control registers are shown in the following table.

Table 1- 18 Saturation control register

Function	Address	Default value	Description
Saturation switch	16'h00f5[5]	1'b0	Saturation control enable 0~enable; 1~disable
Blue saturation	16'h0149	8'he0	Cb saturation gain (/128)
Red saturation	16'h014a	8'he0	Cr saturation gain (/128)

1.19. Contrast

Through linear operation on brightness, changes to image contrast can be realized. The specific register configuration is shown in the following table.

Table 1- 19 Contrast control register

Function	Address	Default value	Description
Contrast switch	16'h00f5[6]	1'b0	Saturation control enable 0~enable; 1~disable
Contrast	16'h014b	8'h48	Contrast coefficient (/64)

2. Electrical Characteristics

Table 2-1 Absolute maximum ratings (to pad)

Item	Symbol	Absolute Maximum Ratings	Unit
Analog supply voltage	V_{AVDD}	-0.3~3.4	V
I/O supply voltage	V_{DOVDD}	-0.3~3.4	V
I/O input voltage	V_I	-0.3 ~ $V_{DOVDD} + 0.3$	V
I/O output voltage	V_O	-0.3 ~ $V_{DOVDD} + 0.3$	V
Operating temperature	T_{OPR}	-30~+85	°C
Functional temperature	T_{SPEC}	-20~+60	°C
Storage temperature	T_{STG}	-40~+85	°C

Table 2-2 DC electrical characteristics (to pad)

Item	Symbol	Min	Typical	Max	Units
Power Supply					
Analog supply voltage	V_{AVDD}	2.7	2.8	2.9	V
I/O supply voltage	V_{DOVDD}	2.7	2.8	2.9	V
Supply Current (Operating current *1, linear mode, 30fps)					
Analog supply current	I_{AVDD}	-	10.7	-	mA
I/O supply current	I_{DOVDD}	-	43.7	-	mA
Total power consumption	Power(*)	-	152.32	-	mW
Digital Input					
Input low level	V_{IL}	-	-	$0.3 \times DOVDD$	V
Input high level	V_{IH}	$0.7 \times DOVDD$	-	-	V
Input capacitor	C_{IN}	-	-	10	pF
Digital Output (25 pF standard load)					
Output high level	V_{OH}	$0.9 \times DOVDD$	-	-	V
Output low level	V_{OL}	-	-	$0.1 \times DOVDD$	V
Serial Interface Input (SCL and SDA)					
Input low level	V_{IL}	- 0.5	0	$0.3 \times DOVDD$	V
Input high level	V_{IH}	$0.7 \times DOVDD$	$DOVDD$	$DOVDD + 0.5$	V

Notes:

1) *1 Operating current: (Typ.) Supply voltage 2.8V/2.8V, $T_j=25^{\circ}\text{C}$;

The light condition: luminous intensity when the sensor outputs 1/3 of the maximum output

Table 2-3 AC characteristics

Item	Symbol	Min	Typical	Max	Unit
AC Parameters					
DC differential linearity deviation	DLE	-	< 1	-	LSB
DC integral linearity deviation	ILE	-	< 2	-	LSB
Crystal and Clock Input					
Input clock frequency	f_{EXTCLK}	6	-	40	MHz
Input clock high pulse width	t_{WH}	5	-	-	ns
Input clock low pulse width	t_{WL}	5	-	-	ns
Input clock duty cycle	-	45	50	55	%

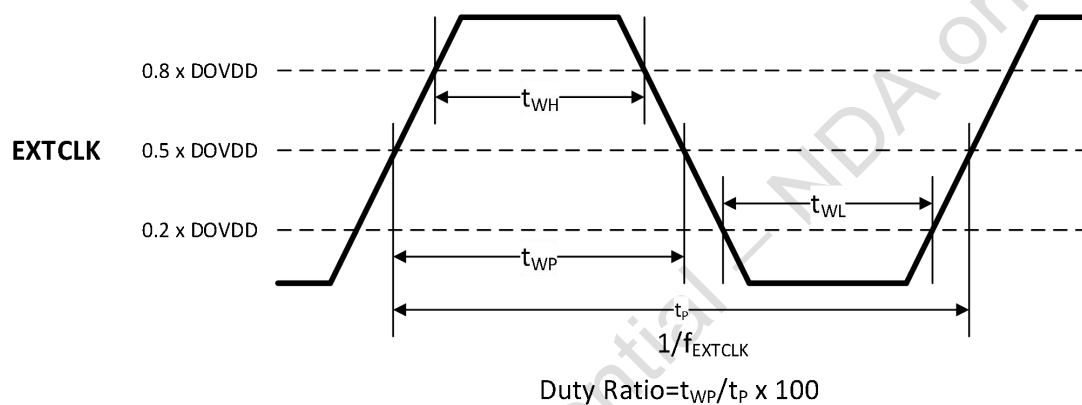


Figure 2-1 Input clock waveform

3. Optical Characteristic

3.1. QE Curve

SC101IoT QE curve is shown below.

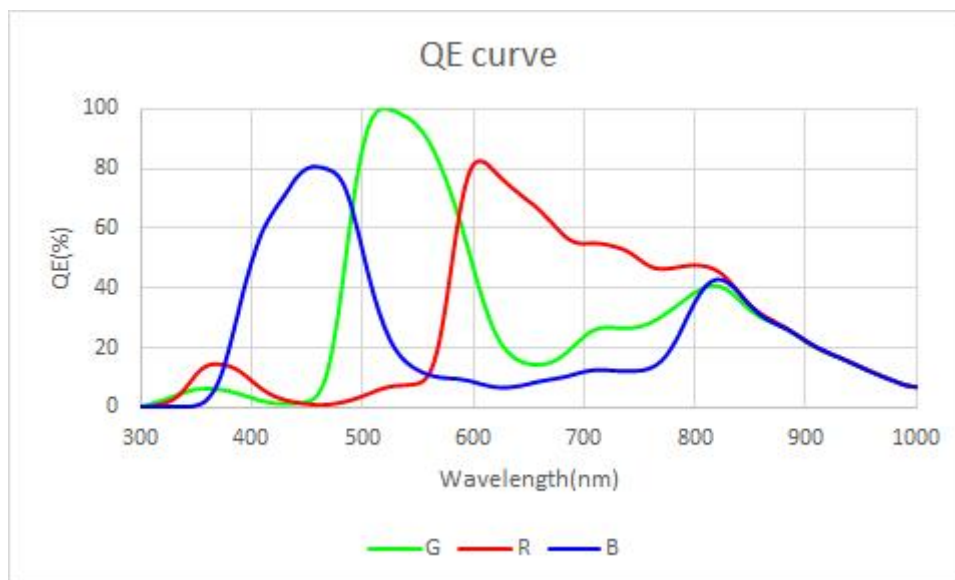


Figure 3-1 QE curve

3.2. Chief Ray Angle (CRA)

SC101IoT CRA curve is shown below.

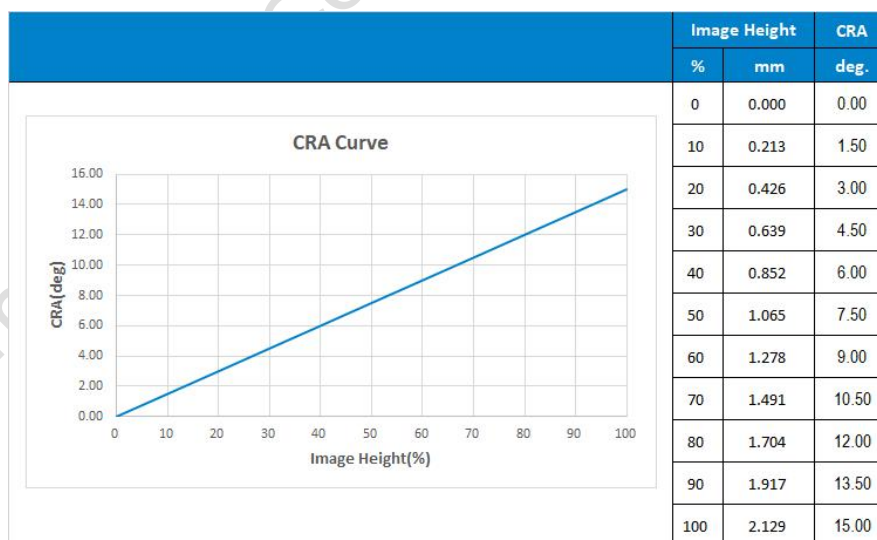


Figure 3-2 CRA curve

4. Packaging Information

SC101IoT provides a 35-pin CSP package. The package drawing is shown in Figure 4-1.

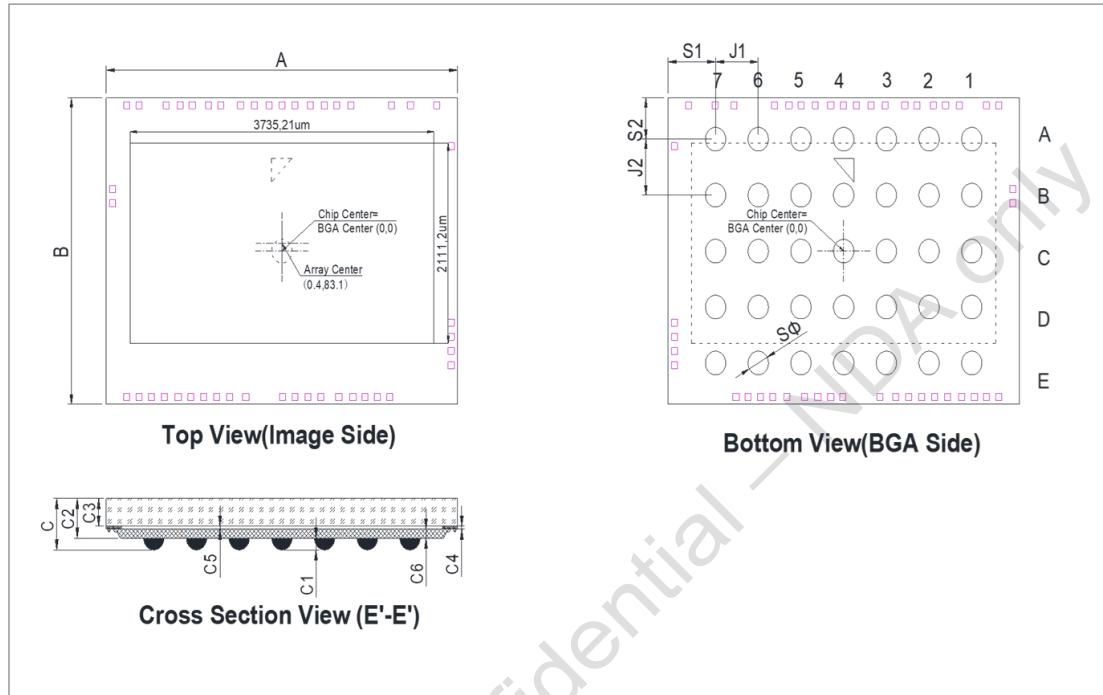


Figure 4-1 Package drawing

Note:

- 1) Chip Center is not coincident with Array Center (Optical Center), Chip Center is not coincident with BGA Center. Taking Chip Center as the origin, the Array Center is (0.4, 83.1), BGA Center is (0, 0), the unit is μm.
- 2) The right angle of the triangle in the Bottom View points to the location of A1, as shown on the figure above. In the Bottom View, the solder ball on the left corner is where A1 locates, the actual location of the triangle shall prevail in kind.

Table 4- 1 Package dimensions

Parameter	Symbol	Nominal	Min	Max	Nominal	Min	Max
		Millimeters			Inches		
Package Body Dimension X	A	4.3180	4.2930	4.3430	0.17000	0.16902	0.17098
Package Body Dimension Y	B	3.2300	3.2050	3.2550	0.12717	0.12618	0.12815
Package Height	C	0.6650	0.6100	0.7200	0.02618	0.02402	0.02835
Cavity wall height	C4	0.0410	0.0370	0.0450	0.00161	0.00146	0.00177
Cavity wall + epoxy thickness (glass to the wafer bonding top point)	C5	0.0435	0.0385	0.0485	0.00171	0.00152	0.00191
Si Thickness	C6	0.1500	0.1400	0.1600	0.00591	0.00551	0.00630
Glass Thickness	C3	0.3000	0.2900	0.3100	0.01181	0.01142	0.01220
Package Body Thickness	C2	0.5350	0.5000	0.5700	0.02106	0.01969	0.02244
Ball Height	C1	0.1300	0.1000	0.1600	0.00512	0.00394	0.00630
Ball Diameter	SΦ	0.2500	0.2200	0.2800	0.00984	0.00866	0.01102
Total Ball Count	N	35	-	-	-	-	-
Ball Count X axis	N1	7	-	-	-	-	-
Ball Count Y axis	N2	5	-	-	-	-	-
Pins Pitch X axis1	J1	0.5250	0.5150	0.5350	0.02067	0.02028	0.02106
Pins Pitch X axis2	J2	0.5900	0.5800	0.6000	0.02323	0.02283	0.02362
BGA ball center to package center offset in X-direction	X	0.0000	-0.0250	0.0250	0.00000	-0.00098	0.00098
BGA ball center to package center offset in Y-direction	Y	0.0000	-0.0250	0.0250	0.00000	-0.00098	0.00098
Edge to Ball Center Distance along X1	S1	0.58400	0.55400	0.61400	0.02299	0.02181	0.02417
Edge to Ball Center Distance along Y1	S2	0.43500	0.40500	0.46500	0.01713	0.01594	0.01831

5. Order Information

Table 5- 1 Order information

Product code	Package	Description
SC101IoT-CS6NN00	35-pin CSP	1.0 Megapixel, RAW/RGB, DVP output

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6. Revision History

Version	Description	Owner and date
0.4	Initial version	Rina Yang/2022.04.02
0.5	Deleted the BT1120 and BT656 functions	Rina Yang/2022.06.16

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