

datasheet

PRELIMINARY SPECIFICATION

1/4" CMOS QXGA (3.2 Megapixel) CameraChip™ sensor
with OmniPixel3™ technology

OV3640

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color CMOS QXGA (3.2 Megapixel) CameraChip™ sensor with OmniPixel3™ technology

datasheet (CSP2) PRELIMINARY SPECIFICATION

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OV3640

color CMOS QXGA (3.2 Megapixel) CameraChip™ sensor with OmniPixel3™ technology

applications

- cellular phones
- toys
- PC multimedia
- digital still camera

ordering information

- **OV03640-VL9A** (color, lead-free)
56-pin CSP2

features

- ultra low power and low cost
- automatic image control functions: automatic exposure control (AEC), automatic white balance (AWB), automatic band filter (ABF), automatic 50/60 Hz luminance detection, and automatic black level calibration (ABLC)
- programmable controls for frame rate, AEC/AGC 16-zone size/position/weight control, mirror and flip, scaling, cropping, windowing, and panning
- image quality controls: color saturation, hue, gamma, sharpness (edge enhancement), lens correction, defective pixel canceling, and noise canceling
- support for output formats: RAW RGB, RGB565/555/444, CCIR656, YUV422/420, YCbCr422 and compression
- support for images sizes: QXGA, and any arbitrary size scaling down from QXGA
- support for video or snapshot operations
- support for horizontal and vertical sub-sampling
- support for data compression output
- support for auto focus control (AFC)
- support for anti-shake
- support for internal and external frame synchronization
- support for LED and flash strobe mode
- standard serial SCCB interface
- digital video port (DVP) parallel output interface
- MIPI serial output interface
- support for second camera chip-sharing ISP and MIPI interface
- embedded microcontroller
- embedded one-time programmable (OTP) memory
- on-chip phase lock loop (PLL)
- programmable I/O drive capability

key specifications

- **active array size:** 2048 x 1536
- **power supply:**
 - core: 1.5VDC $\pm$ 5%
 - analog: 2.5 ~ 3.0V
 - I/O: 1.7 ~ 3.0V
- **power requirements:**
 - active: TBD
 - standby: TBD
- **temperature range:**
 - operating: -20°C to 70°C
 - stable image: 0°C to 50°C
- **output formats (8-bit):** YUV(422/420) / YCbCr422, RGB565/555/444, CCIR656, 8-bit compression data, 8-/10-bit raw RGB data
- **lens size:** 1/4"
- **lens chief ray angle:** 25° non-linear (see [Table 10-1](#))
- **input clock frequency:** 6 ~ 27 MHz
- **maximum image transfer rate:**
 - QXGA (2048x1536): 15fps for QXGA and any size scaling down from QXGA
 - XGA (1024x768): 30fps for XGA and any size scaling down from XGA
- **sensitivity:** TBD
- **S/N ratio:** TBD
- **dynamic range:** TBD
- **shutter:** rolling shutter
- **scan mode:** progressive
- **maximum exposure interval:** 1560 x t_{ROW}
- **gamma correction:** programmable
- **pixel size:** 1.75 μm x 1.75 μm
- **well capacity:** TBD
- **dark current:** TBD
- **fixed pattern noise (FPN):** TBD
- **image area:** 3626 μm x 2709 μm
- **package dimensions:** 6285 μm x 6125 μm

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV3640 image sensor. The package information is shown in **section 9**.

table 1-1 signal descriptions (sheet 1 of 3)

pin number	signal name	pin type	description	default I/O status
A1	HREF	I/O	horizontal reference output	input
A2	AVDD	power	analog power	
A3	STROBE	I/O	strobe output or scan chain test mode input	input
A4	SVDD	power	analog power	
A5	PWDN	input	power down active high with internal pull-down resistor	
A6	SDA	I/O	SCCB data	
A7	SCL	input	SCCB input clock	
A8	VREFN	reference	internal analog reference	
A9	GPIO1	I/O	general purpose I/O (GPIO) 1	input
B1	DATA8	I/O	digital video port (DVP) bit[8]	input
B2	AGND	ground	ground for analog circuit	
B3	VSYNC	I/O	vertical sync output	input
B4	FREX	I/O	anti-shake status output or OTP memory output	input
B5	SGND	ground	ground for sensor circuit	
B6	RESET_B	input	reset (active low with internal pull-up resistor)	
B7	VREFH	reference	internal analog reference	
B8	EGND	ground	ground for MIPI core	
B9	MDN1	output	MIPI first data lane negative output	
C1	DATA6	I/O	digital video port (DVP) bit[6]	input
C2	DATA7	I/O	digital video port (DVP) bit[7]	input
C3	DATA9	I/O	digital video port (DVP) bit[9]	input
C7	XVCLK	input	system input clock	
C8	EGND	ground	ground for MIPI core	

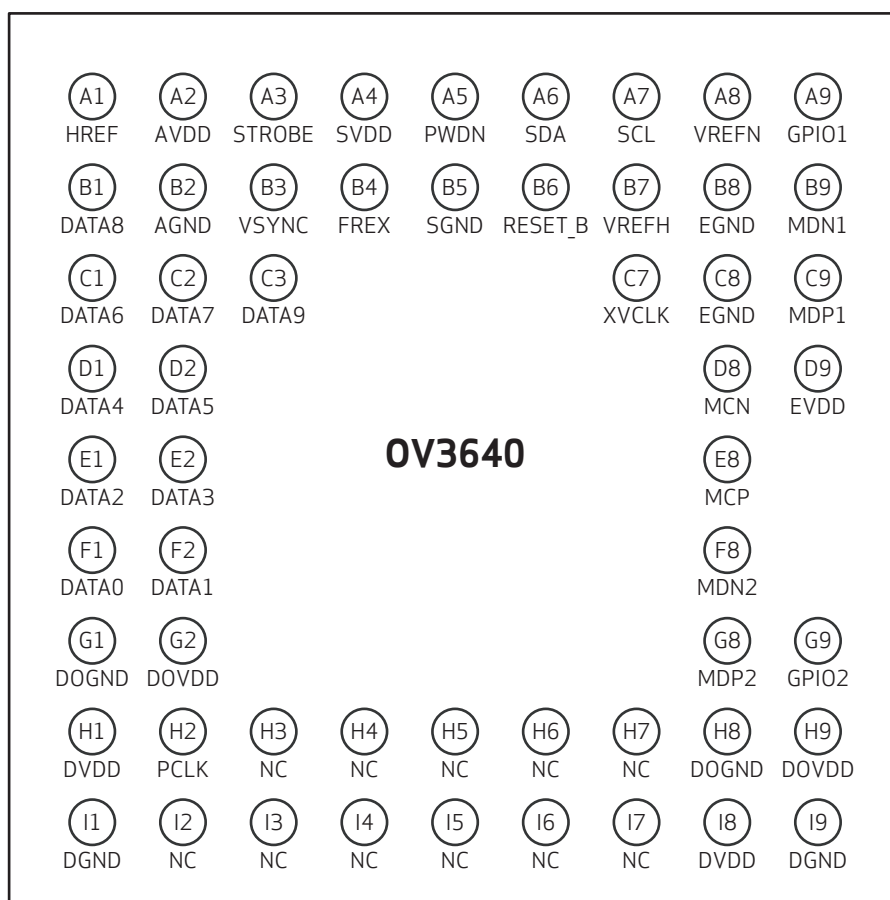
table 1-1 signal descriptions (sheet 2 of 3)

pin number	signal name	pin type	description	default I/O status
C9	MDP1	output	MIPI first data lane positive output	
D1	DATA4	I/O	digital video port (DVP) bit[4]	input
D2	DATA5	I/O	digital video port (DVP) bit[5]	input
D8	MCN	output	MIPI clock lane negative output	
D9	EVDD	reference	power for MIPI core	
E1	DATA2	I/O	digital video port (DVP) bit[2]	input
E2	DATA3	I/O	digital video port (DVP) bit[3]	input
E8	MCP	output	MIPI clock lane positive output	
F1	DATA0	I/O	digital video port (DVP) bit[0]	input
F2	DATA1	I/O	digital video port (DVP) bit[1]	input
F8	MDN2	output	MIPI second data lane negative output	
G1	DOGND	ground	ground for I/O circuit	
G2	DOVDD	power	power for I/O circuit	
G8	MDP2	output	MIPI second data lane positive output	
G9	GPIO2	I/O	general purpose I/O (GPIO) 2	input
H1	DVDD	reference	power for digital core	
H2	PCLK	I/O	pixel clock output	input
H3	NC	–	no connect	–
H4	NC	–	no connect	–
H5	NC	–	no connect	–
H6	NC	–	no connect	–
H7	NC	–	no connect	–
H8	DOGND	ground	ground for I/O circuit	
H9	DOVDD	power	power for I/O circuit	
I1	DGND	ground	ground for digital core	
I2	NC	–	no connect	–
I3	NC	–	no connect	–
I4	NC	–	no connect	–
I5	NC	–	no connect	–
I6	NC	–	no connect	–

table 1-1 signal descriptions (sheet 3 of 3)

pin number	signal name	pin type	description	default I/O status
I7	NC	–	no connect	–
I8	DVDD	reference	power for digital core	–
I9	DGND	ground	ground for digital core	–

figure 1-1 pin diagram



3640_CSP_DS_1.1

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2 system level description

2.1 overview

The OV3640 (color) CameraChip™ sensor is a low voltage, high performance 1/4-inch 3.2 megapixel CMOS image sensor that provides the full functionality of a single chip QXGA (2048x1536) camera using OmniPixel3™ technology in a small footprint package. It provides full-frame, sub-sampled, windowed or arbitrarily scaled 8-bit/10-bit images in various formats via the control of the Serial Camera Control Bus (SCCB) interface or MIPI interface.

The OV3640 has an image array capable of operating at up to 15 frames per second (fps) in QXGA resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control, defective pixel canceling, noise canceling, etc., are programmable through the SCCB interface, MIPI interface or embedded microcontroller. The OV3640 also includes a compression engine for increased processing power. In addition, Omnivision CameraChip sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

The OV3640 has an embedded a microcontroller, which can be combined with an internal auto focus engine and programmable general purpose I/O modules (GPIO), for external auto focus control. It also provides an anti-shake function with an internal anti-shake engine. For storage purposes, the OV3640 also includes a one-time programmable (OTP) memory.

The OV3640 supports both a digital video parallel port and a serial MIPI port. The MIPI and ISP interface can be used for a second camera sensor without requiring a dual serial port camera system.

2.2 architecture

The OV3640 sensor core generates stream pixel data at a constant frame rate, indicated by HREF and VSYNC.

figure 2-1 shows the functional block diagram of the OV3640 image sensor. **figure 2-2** shows an example application using an OV3640 sensor.

The timing generator outputs signals to access the rows of the image array, precharging and sampling the rows of array in series. In the time between pre-charging and sampling a row, the charge in the pixels decreases with the time exposed to the incident light. This is known as exposure time.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs 10-bit data for each pixel in the array.

figure 2-1 OV3640 block diagram

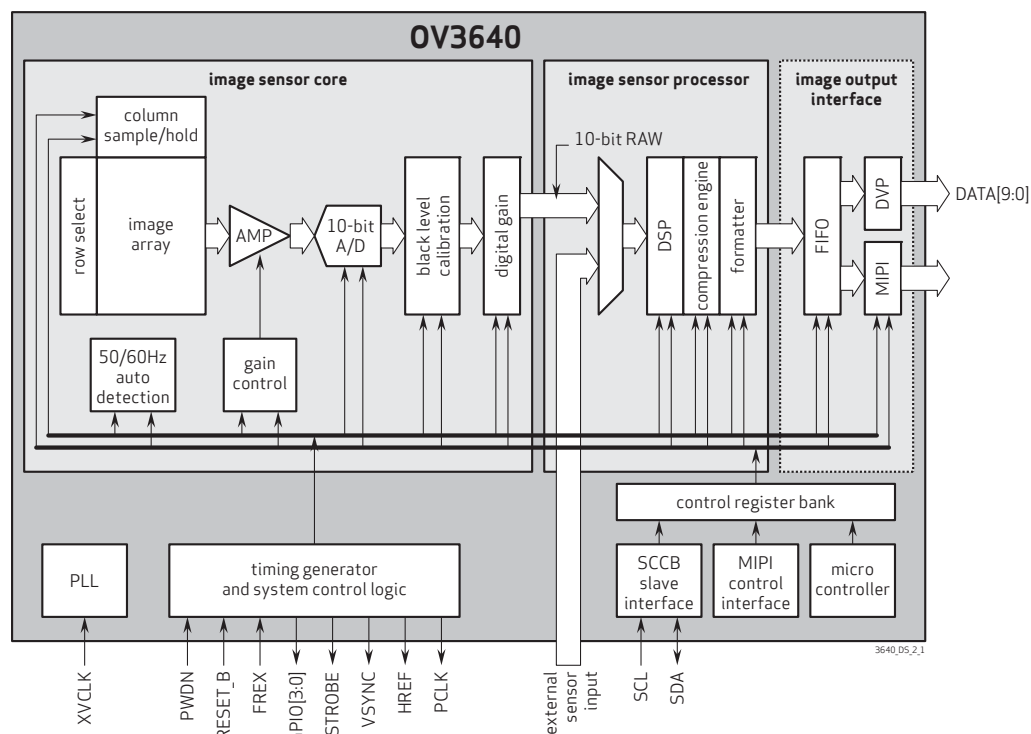
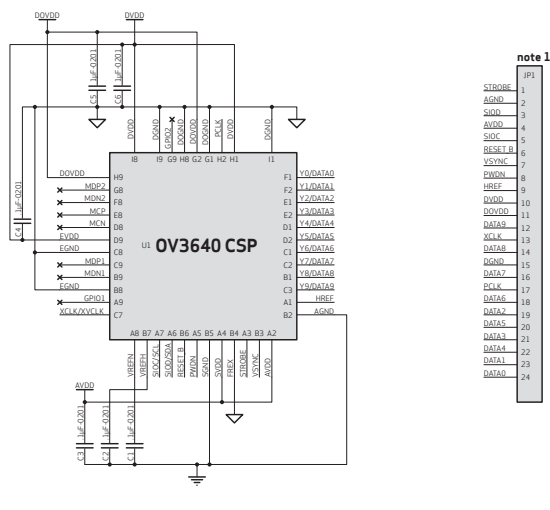


figure 2-2 reference design schematic



note 1 flex cable to Molex 52437-2491

note 2 PWDN should be connected to ground outside of module if unused.
RESET_B should be connected to DOVDD outside of module if unused.
AVDD is 2.45V +/- 10% of sensor analog power (clean).
DOVDD is 1.5V +/- 10% of sensor digital power (clean).
DOVDD is 1.7V - 3.0V of sensor digital I/O power (clean).
sensor AGND and DGND should be separated and connected to a single point outside the PCB (do not connect inside the module).
capacitors should be close to the related sensor pins.
DATA[9:0] is the sensor's 10-bit RGB output (DATA[9]: MSB; DATA[0]: LSB).

3640_CSP_DS_2.2

2.3 I/O control

The OV3640 I/O pad direction and driving capability can be easily adjusted. **table 2-1** lists the driving capability and direction control registers of the I/O pads.

table 2-1 driving capability and direction control for I/O pads

function	register	description
output driving capability control	0x30B2[1:0]	R_PAD[1:0]: Output driving capability 00: 1x 01: 2x 10: 3x 11: 4x
DATA[9:0] I/O control	{0x30B1[1:0], 0x30B0[7:0]}	Input/Output selection for the DATA[9:0] pins: 0: Input 1: Output
GPIO2 I/O control	0x30B1[7]	Input/Output selection for the GPIO2 pin: 0: Input 1: Output
GPIO1 I/O control	0x30B1[6]	Input/Output selection for the GPIO1 pin: 0: Input 1: Output
VSYNC I/O control	0x30B1[5]	Input/Output selection for the VSYNC pin: 0: Input 1: Output
HREF I/O control	0x30B1[2]	Input/Output selection for the HREF pin: 0: Input 1: Output
PCLK I/O control	0x30B1[3]	Input/Output selection for the PCLK pin: 0: Input 1: Output
STROBE I/O control	0x30B1[4]	Input/Output selection for the STROBE pin: 0: Input 1: Output

2.4 system clock control

The OV3640 PLL allows for an input clock frequency ranging from 6~27 Mhz and has a maximum VCO frequency of 1.3 Ghz. SysClk is the input clock for the sensor core, SerClk is for the MIPI and DvpClk is for the internal clock of the Image Signal Processing (ISP) block. The PLL can be bypassed by setting register 0x300F[3] to 1.

2.5 SCCB interface

The Serial Camera Control Bus (SCCB) interface controls the CameraChip sensor operation. Refer to the OmniVision Technologies Serial Camera Control Bus (SCCB) Specification for detailed usage of the serial control port.

2.6 power up sequence

Powering up the OV3640 sensor does not require a special power supply sequence. The sensor includes an on-chip initial power-up reset feature. It will reset the whole chip during power up. Manually applying a hard reset upon power up is recommended even though the on-chip power-up reset is included.

2.7 reset

The OV3640 sensor includes a RESET_B pin that forces a complete hardware reset when it is pulled low (GND). The OV3640 clears all registers and resets them to their default values when a hardware reset occurs. A reset can also be initiated through the SCCB interface by setting register 0x3012[7] to high.

2.8 standby and sleep

Two suspend modes are available for the OV3640:

- hardware standby
- SCCB software sleep

To initiate hardware standby mode, the PWDN pin must be tied to high. When this occurs, the OV3640 internal device clock is halted and all internal counters are reset and registers are maintained.

Executing a software power-down through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

The OV3640 also supports MIPI ultra low power state (ULPS). After receiving ULPS command from host, the OV3640 will enter into ULPS mode. Except for the low speed part of the MIPI PHY and SCCB, all other blocks enter into power down mode in ULPS mode.

3 block level description

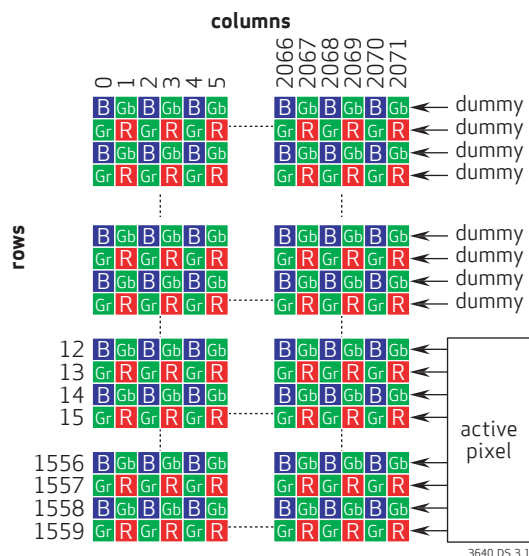
3.1 pixel array structure

The OV3640 sensor has an image array of 2072 columns by 1568 rows (3,248,896 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 3,248,896 pixels, 3,145,728 (2048x1536) are active pixels and can be output. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

figure 3-1 sensor array region color filter layout



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4 image sensor core digital functions

4.1 mirror and flip

The OV3640 provides Mirror and Flip readout modes, which respectively reverse the sensor data readout order horizontally and vertically (see [figure 4-1](#)). In mirror, since the Bayer order changes from BGBG... to GBGB..., the OV3640 usually delays the readout sequence by one pixel by setting register 0x397C[1] to 1. In flip, the OV3640 does not need additional settings because the ISP block will auto-detect whether the pixel is in the red line or blue line and make necessary adjustment.

figure 4-1 mirror and flip samples

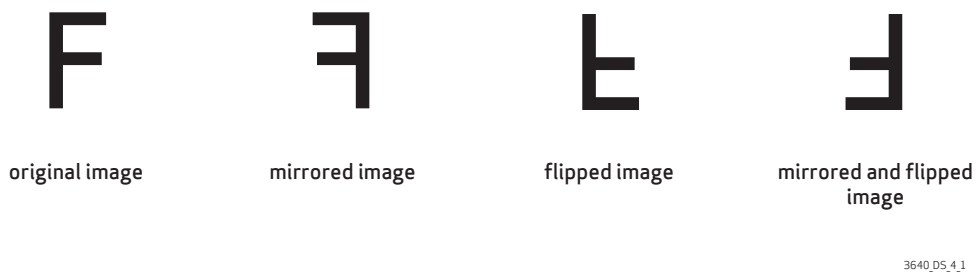


table 4-1 mirror and flip function control

function	register	description
mirror	0x307C[1]	Mirror ON/OFF select 0: Mirror OFF 1: Mirror ON
	0x3090[3]	Array mirror ON/OFF select 0: Array mirror OFF 1: Array mirror ON
flip	0x307C[0]	Flip ON/OFF select 0: Flip OFF 1: Flip ON
	0x3023	B/R row adjustment

4.2 image cropping

An image cropping area is defined by four parameters, HS(horizontal start), HW(horizontal width), VS(vertical start), VH(vertical height). By properly setting the parameters, any portion within the sense array size can be cropped as a visible area. This cropping is achieved by simply masking the pixels outside the cropping window; thus, it will not affect original timings. It will also not conflict with the flip and mirror functions.

figure 4-2 image cropping

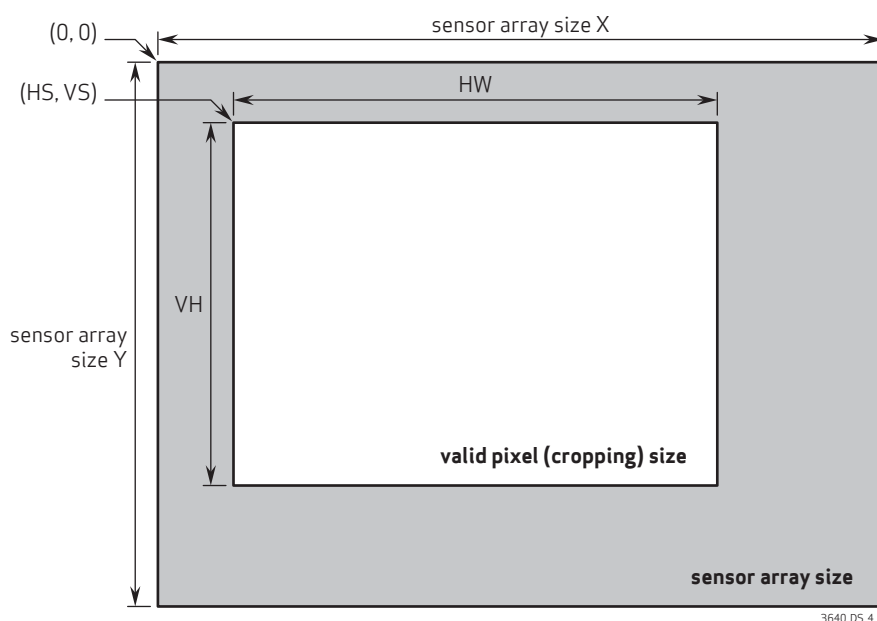


table 4-2 image cropping control functions

function	register	description
horizontal start	{0x3020, 0x3021}	HS[15:8] = 0x3020 HS[7:0] = 0x3021
vertical start	{0x3022, 0x3023}	VS[15:8] = 0x3022 VS[7:0] = 0x3023
horizontal width	{0x3024, 0x3025}	HW[15:8] = 0x3024 HW[7:0] = 0x3025
vertical height	{0x3026, 0x3027}	VH[15:8] = 0x3026 VH[7:0] = 0x3027

4.3 test pattern

For testing purposes, the OV3640 offers one type of test pattern, CBAR.

figure 4-3 test pattern

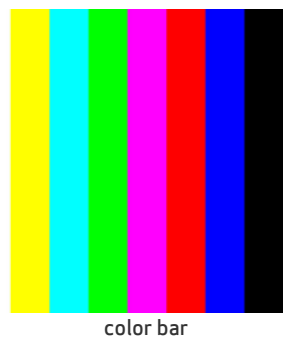


table 4-3 test pattern selection control

function	register	description
test pattern ON/OFF	0x3080[7]	Test pattern ON/OFF select 0: OFF 1: ON
color bar	0x307B[1:0]	color bar pattern select 10: Color bar pattern
	0x307D[7]	color bar enable 0: Color bar OFF 1: Color bar enable
	0x306C[4]	0: Color bar 1: Normal image

4.4 50/60hz detection

When the integration time is not an integer multiple of the period of light intensity, the image will flicker. The function of the detector is to detect whether the sensor is under a 50hz or 60hz light source so that the basic step of integration time can be determined.

4.5 AEC/AGC algorithms

The Auto Exposure Control (AEC) and Auto Gain Control (AGC) allows the CameraChip sensor to adjust the image brightness to a desired range by setting the proper exposure time and gain applied to the image. Besides automatic control, exposure time and gain can be set manually from external control.

4.6 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines. These lines are used to provide the data for black level calibration.

4.7 strobe flash control

To achieve the best image quality possible in low light conditions, the use of a strobe flash is recommended. The OV3640 provides a programmable strobe signal function.

4.7.1 sensor-controlled strobe flash

The OV3640 can generate a programmable strobe signal from the Strobe pin (pin 04). [table 4-4](#) lists the strobe pulse control registers.

table 4-4 strobe control functions

function	register	description
strobe function enable	0x307A [7]	Strobe function enable 0: Strobe disable 1: Start strobe enable
strobe output pulse polarity control	0x307A [6] (TMC4[6])	Strobe output polarity control 0: Positive pulse 1: Negative pulse
xenon mode strobe pulse width	0x307A [3:2] (TMC4[3:2])	Xenon mode pulse width 00: 1 line 01: 2 lines 10: 3 lines 11: 4 lines
strobe mode	0x307A [1:0] (TMC4[1:0])	Strobe mode select 00: Xenon mode 01: LED 1 & 2 mode 10: LED 1 & 2 mode 11: LED 3 mode

4.7.1.1 strobe pulse

The strobe signal is programmable. It supports both LED and Xenon mode. The polarity of the pulse can be changed. The strobe signal is enabled (turned high / low depending on the pulse's polarity) by requesting the signal via the SCCB. Flash modules are typically triggered to the rising edge (falling edge, if signal polarity is changed). It supports the flashlight modes shown in [table 4-5](#).

table 4-5 flashlight modes

function	register	description
xenon	one pulse	no
LED 1	pulse	no
LED 2	pulse	no
LED 3	continuous	yes

4.8 one time programmable (OTP) memory

The OV3640 supports 128 bits maximum one-time programmable (OTP) memory to store chip identification and manufacturing information. Contact your local OmniVision FAE for more details.

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5 image sensor processor digital functions

5.1 lens correction (LENC)

The main purpose of the LENC function is to compensate for lens imperfection. According to the radius of each pixel to the lens, the module calculates a gain for the pixel, correcting each pixel with its gain calculated to compensate for the light distribution due to lens curvature.

5.2 auto white balance (AWB)

The main purpose of the Auto White Balance (AWB) function is to automatically correct the white balance of the image. It supports manual white balance, simple AWB and advanced AWB. For advanced AWB settings, contact your local OmniVision FAE.

5.3 gamma curve (GMA)

The main purpose of the Gamma (GMA) function is to compensate for the non-linear characteristics of the sensor. GMA converts the pixel values according to the Gamma curve to compensate the sensor output under different light strengths. The non-linear gamma curve is approximately constructed with different linear functions.

5.4 white black pixel cancellation (WBC)

The main purpose of White/Black pixel Cancellation (WBC) function is to remove the white/black pixels effect.

table 5-1 WBC-related registers

register address	register name	function
0x3301	DSP_CTRL_2	DSP Control 1
		Bit[2]: WC_en This function removes the white pixels introduced by the sensor's defects.
		Bit[1]: BC_en This function removes the black pixels introduced by the sensor's defects.

5.5 interpolation/de-noise/edge enhancement (CIP)

The CIP functions include de-noising of raw images, RAW to RGB interpolation, and edge enhancement. CIP functions work in both manual and auto modes.

5.6 color matrix (CMX)

The main purpose of the Color Matrix (CMX) function is to convert images from the RGB domain to YUV domain. For different color temperatures, the parameters in the transmitting function will be changed.

5.7 zoom out (ZOOM)

The main purpose of the Zoom out (ZOOM) function is to zoom out the image. According to the new_width and new_height of the new image, the module uses several pixels' values to generate one pixel's value. Some pixels' values are divided and used in two or more adjacent pixels. Calculating the algorithm uses finite float point to keep the mantissa when using this function.

5.8 special digital effects (SDE)

The Special Digital Effects (SDE) functions include hue/saturation control, brightness, contrast, etc. Use SDE_CTRL to add some special effects to the image. Calculate the new U and V from Hue Cos, Hue Sin, and parameter signs. Saturate U and V using the Sat_u and Sat_v registers. Calculate Y using Y offset, Y gain, and Ybright or set the Y value. SDE supports negative, black/white, sepia, greenish, blueish, redish and other image effects which combine the effects already listed.

5.9 overlay

The OV3640 supports an overlay function.

5.10 autofocus (AFC)

AFC has three required functions:

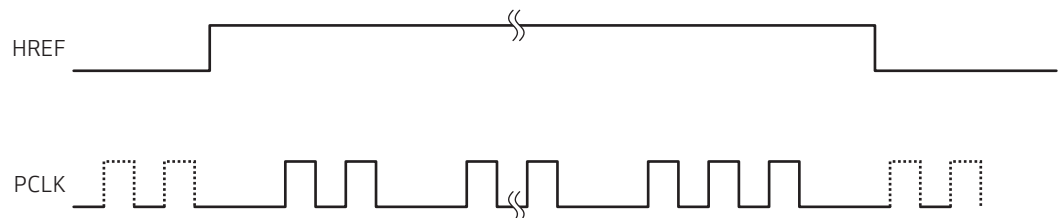
- Local Statistics - calculate maximum, minimum, and mean separately for R, G, and B in nine programmable zones
- Histograms - calculates intensity histograms of R, G, and B pixels separately in at least three different programmable zones
- Edge information - collects edge information for at least sixteen programmable zones

Contact your local OmniVision FAE for further details.

5.11 compression engine

5.11.1 compression mode 1 timing

figure 5-1 compression mode 1 timing



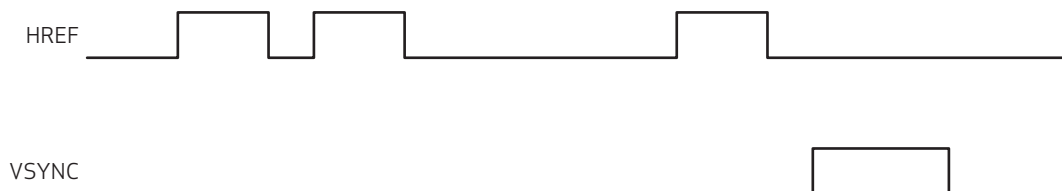
note 1 the whole frame has only one HREF
PCLK will be gated when there is no image data to transmit

3640_DS_5_5

5.11.2 compression mode 2 timing

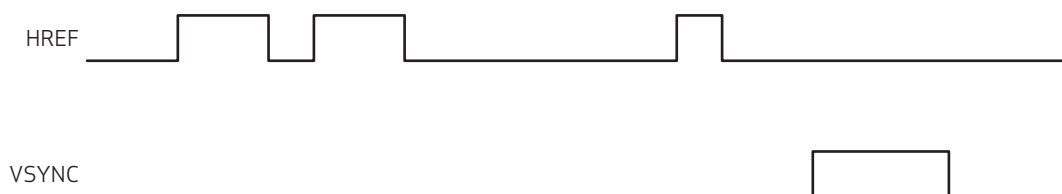
figure 5-2 compression mode 2 timing

a) dummy data padding at the last line



note 1 compression data is output with programmable width, the last line may contain dummy data to match the width. in each frame, the line numbers are different.

b) no dummy data padding at the last line



note 1 compression data is output with programmable width, the last line may be less than others (there is no dummy data). in each frame, the line numbers are different.

3640_05_5_1

5.12 MCU description

Microprocessor firmware can be downloaded by writing to registers starting from 0x8000. A total of 6 kB of program memory can be used for program storage. Before downloading the firmware, the user must enable the MCU clock.

5.13 format description

Format control converts internal data format into the desirable output format including YUV, RGB, raw, compression data, CCIR656, HSYNC mode, etc.

table 5-2 format control register list (sheet 1 of 3)

register address	register name	function
0x3400	FMT_MUX_CTRL0	FMT_MUX_CTRL0 Bit[2:0]: Format input source select 000: DSP YUV444 001: DSP RGB888 010: DSP YUV422 011: DSP raw 100: Internal CIF raw 101: External CIF raw 110: External CIF YUV422 bypass 111: Not used
0x3403	ISP_PAD_CTRL2	ISP_PAD_CTRL2 Bit[7:4]: Xstart - x start address for DVP windowing Bit[3:0]: Ystart - y start address for DVP windowing

table 5-2 format control register list (sheet 2 of 3)

register address	register name	function
0x3404	FMT_CTRL00	FMT_CTRL00 Bit[7]: UV_sel 0: Use UV_avg, Y 1: Use U0Y0, V0Y1 Bit[6]: YUV422_in Bit[5:0]: YUV422: 0x00: yuyvyuyv.../yuyvyuyv... 0x01: yvyuyvyu.../yvyuyvyu... 0x02: uyvyuyvy.../uyvyuyvy... 0x03: vyuyvyuy.../vyuyvyuy... YUV420: 0x04: yyyy.../yuyvyuyv... 0x05: yyyy.../yvyuyvyu... 0x06: yyyy.../uyvyuyvy... 0x07: yyyy.../vyuyvyuy... 0x08: yuyvyuyv.../yyyy... 0x09: yvyuyvyu.../yyyy... 0x0A: uyvyuyvy.../yyyy... 0x0B: vyuyvyuy.../yyyy... 0x0C: uyuyuy.../vyvyvy Y8: 0x0D: yyyy.../yyyy... YUV444 (RGB888) 0x0E: yuvyuv.../yuvyuv... (gbrgrb.../gbrgrb...) 0x0F: yvuyvu.../yvuyvu... (grbgrb.../grbgrb...) 0x1C: uyvyuv.../uyvyuv... (bgrbgr.../bgrbgr...) 0x1D: vyuyvu.../vyuyvu... (rgbrgb.../rgbrgb...) 0x1E: uyvyuv.../uyvyuv... (brgbrg.../brgbrg...) 0x1F: yuvyuv.../yuvyuv... (rbgrbg.../rbgrbg...) RGB565: 0x10: {b[4:0],g[5:3]}, {g[2:0],r[4:0]} 0x11: {r[4:0],g[5:3]}, {g[2:0],b[4:0]} 0x30: {g[2:0],b[4:0]}, {r[4:0],g[5:3]} (MIPI RGB565) RGB555: 0x12: {b[4:0],g[4:2]}, {g[1:0],1'b0,r[4:0]} 0x13: {r[4:0],g[4:2]}, {g[1:0],1'b0,b[4:0]} 0x32: {g[1:0],1'b0,b[4:0]}, {r[4:0],g[4:2]} RGB444: 0x14: {b[3:0],1'b0,g[3:1]}, {g[0],2'h0,r[3:0],1'b0} 0x15: {r[3:0],1'b0,g[3:1]}, {g[0],2'h0,b[3:0],1'b0} 0x34: {g[0],2'h0,b[3:0],1'b0}, {r[3:0],1'b0,g[3:1]} (MIPI RGB444) 0x37: {4'b0,r[3:0]}, {g[3:0],b[3:0]} 0x38: {4'b0,b[3:0]}, {g[3:0],r[3:0]} 0x16: {b[3:0],g[3:0]}, {r[3:0],b[3:0]} ... 0x17: {r[3:0],g[3:0]}, {b[3:0],r[3:0]} ... RAW: 0x18: bgbg.../grgr... 0x19: gbgb.../rgrg... 0x1A: grgr.../bgbg... 0x1B: rgrg.../gbgb...

table 5-2 format control register list (sheet 3 of 3)

register address	register name	function
		DITHER_CTRL0
		Bit[6]: Dither_sel
		0: Use register setting
		1: Dithering according to fmt_control
		Bit[5:4]: R_dithering
		00: No dithering
		01: 4 bit
		10: 5 bit
		11: 6 bit
0x3405	DITHER_CTRL0	Bit[3:2]: G_dithering
		00: No dithering
		01: 4 bit
		10: 5 bit
		11: 6 bit
		Bit[1:0]: B_dithering
		00: No dithering
		01: 4 bit
		10: 5 bit
		11: 6 bit

6 image sensor output interface digital functions

6.1 digital video port (DVP)

6.1.1 overview

The Digital Video Port (DVP) provides 10-bit parallel data output in all formats supported and extended features including compression mode, CCIR656 format, HSYNC mode and test pattern output.

6.1.2 DVP timing

figure 6-1 DVP timing diagram

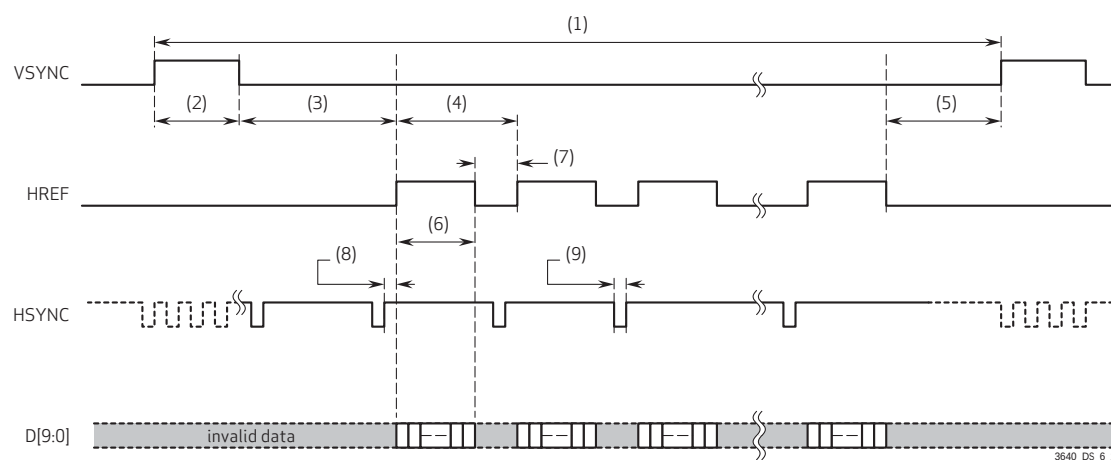


table 6-1 DVP timing specifications (sheet 1 of 2)

mode	timing
QXGA 2048x1536	(1) 3725568 tp $\cong$ 1568 tline (2) 2048 tp (4 tline = $2376 \times 4 = 9504$ tp in HSYNC mode) (3) 28724 tp (4) 2376 tp (5) 45588 tp (6) 2048 tp (7) 328 tp (8) 0 tp (9) 328 tp



note

The timing values shown in **table 6-1** may vary depending upon register settings.

table 6-1 DVP timing specifications (sheet 2 of 2)

mode	timing
UXGA 1600x1200	(1) 2901177 tp $\cong$ 1221 tline (2) 2048 tp (3) 31638 tp (4) 2376 tp (5) 17067 tp (6) 1600 tp (7) 776 tp (8) 0 tp (9) 776 tp
XGA 1024x768 (PCLK/2)	(1) 1849715 tp $\cong$ 779 tline (2) 2048 tp (4 tline = 2376 x 4 = 9504 tp in HSYNC mode) (3) 15787 tp (4) 2376 tp (5) 8464 tp (6) 1024 tp (7) 1352 tp (8) 0 tp (9) 1352 tp
SQCIF 128x96 (PCLK/14)	(1) 264300 tp $\cong$ 97 tline (2) 2048 tp (3) 2967 tp (4) 2716 tp (5) 1137 tp (6) 128 tp (7) 2588 tp (8) 0 tp (9) 2588 tp

6.1.3 DVP image formats

6.1.3.1 YUV422 format

Uncompressed YUV422 data is sent out through DATA[9:2] and the sequence can be YUYV, UYVY, YVYU, VYUY.

table 6-2 YUYV format

DATA[9:2]	first pixel	first pixel	second pixel	second pixel	third pixel	third pixel
even	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]
odd	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]

table 6-3 UYVY format

DATA[9:2]	first pixel	first pixel	second pixel	second pixel	third pixel	third pixel
even	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]
odd	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]

table 6-4 YVYU format

DATA[9:2]	first pixel	first pixel	second pixel	second pixel	third pixel	third pixel
even	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]
odd	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]

table 6-5 VYUY format

DATA[9:2]	first pixel	first pixel	second pixel	second pixel	third pixel	third pixel
even	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]
odd	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]

6.1.3.2 YUV420 format

The data format of uncompressed YUV420 is similar to that of uncompressed YUV422 except that UV data of either even or odd lines is dropped by de-asserting PCLK.

6.1.3.3 Y8 format

Uncompressed Y8 data is sent out through DATA[9:2]. The frequency of PCLK is the same as that of raw data or half of YUV422/420.

6.1.3.4 RGB565 format

Uncompressed RGB565 data is sent out through DATA[9:2].

table 6-6 RGB565 format

bytes	D9	D8	D7	D6	D5	D4	D3	D2
even	R7	R6	R5	R4	R3	G7	G6	G5
odd	G4	G3	G2	B7	B6	B5	B4	B3

6.1.3.5 RGB555 format

table 6-7 RGB555 format

bytes	D9	D8	D7	D6	D5	D4	D3	D2
even	R7	R6	R5	R4	R3	G7	G6	G5
odd	G4	G3	0	B7	B6	B5	B4	B3

6.1.3.6 RGB444 format

The data format of uncompressed RGB444 is similar to RGB565 except that the lowest bit of R, B, and the lowest 2 bits of G are dummy bits.

table 6-8 RGB444 format

bytes	D9	D8	D7	D6	D5	D4	D3	D2
even	X	X	X	X	R7	R6	R5	R4
odd	G7	G6	G5	G4	B7	B6	B5	B4

6.2 mobile industry processor interface (MIPI)

MIPI provides a single uni-directional clock lane and two bi-directional data lane solution for communication links between components inside a mobile device. Two data lanes have full support for HS(uni-direction) and LP (bi-directions) data transfer mode. Contact your local OmniVision FAE for more details.

7 register tables

The following tables provide descriptions of the device control registers contained in the OV3640. For all registers enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x78 for write and 0x79 for read.

table 7-1 system control registers (sheet 1 of 9)

address	register name	default value	R/W	description
0x3000	AGC[15:8]	0x00	RW	Auto Gain Control Bit[7:0]: AGC RSVD gain register
0x3001	AGC[7:0]	0x00	RW	Auto Gain Control - AGC[7:0] Bit[7:0]: Actual Gain – Range from 1x to 32x $\text{Gain} = (\text{Bit}[7]+1) \times (\text{Bit}[6]+1) \times (\text{Bit}[5]+1) \times (\text{Bit}[4]+1) \times (1+\text{Bit}[3:0]/16)$ Set Auto1[2] (R0x3013[2]) = 0 to disable AGC.
0x3002	AEC[15:8]	0x00	RW	Auto Exposure Control - AEC[15:8]
0x3003	AEC[7:0]	0x01	RW	Auto Exposure Control - AEC[7:0] AEC[15:0]: Exposure time $\text{Tex} = \text{Tline} \times \text{AEC}[15:0]$ $\text{Tline} \leq \text{Tex} \leq 1 \text{ frame period}$ The maximum exposure time will be 1 frame period even if Tex is set longer than 1 frame period. Set Auto1[0] (R0x3013[0]) = 0 to disable AEC.
0x3004	AECL[7:0]	0x00	RW	Manual Extreme Bright Exposure Control - AECL[7:0] In extremely bright conditions where Tex must be less than Tline, the exposure time may be set manually by this control. $\text{Tex} = \text{Tline} - \text{L1AEC}[7:0] \text{ steps}$ $\text{Tex min.} \leq \text{Tex} \leq \text{Tline}$ Set Auto2[1] (R0x3014[1]) = 1 to enable manual AECL.
0x3005	RED[7:0]	0x40	RW	AWB Red Gain
0x3006	GREEN[7:0]	0x40	RW	AWB Green Gain
0x3007	BLUE[7:0]	0x40	RW	AWB Blue Gain
0x3008~ 0x3009	RSVD	–	–	Not used
0x300A	PIDH	0x36	RW	Product ID MSBs (read only)
0x300B	PIDL	0x40	RW	Product ID LSBs (read only)
0x300C	SCCB ID	0x78	RW	SCCB ID

table 7-1 system control registers (sheet 2 of 9)

address	register name	default value	R/W	description
0x3011	CLK[7:0]	0x00	RW	Clock Rate Control Bit[7]: Digital frequency doubler 0: OFF 1: ON Bit[6]: PLL and clock divider bypass 0: Master mode, sensor provides PCLK 1: Slave mode, external PCLK input from XCLK1 pin Bit[5:0]: Clock divider CLK = XCLK1/(decimal value of CLK[5:0] + 1)
0x3012	SYS[7:0]	0x00	RW	Format Control Bit[7]: SRST 1: Initiates soft reset. All registers are set to factory default values after which the chip resumes normal operation Bit[6:4]: Sensor array resolution 000: QXGA (full size) mode 001: XGA mode Bit[3]: CC656 protocol on/off (not used) Bit[2:0]: Output format selection (not used)

table 7-1 system control registers (sheet 3 of 9)

address	register name	default value	R/W	description
0x3013	AUTO_1[7:0]	0xE7	RW	Auto Control 1
				Bit[7]: AEC speed selection 0: Normal 1: Faster AEC correction
				Bit[6]: AEC speed/step selection 0: Small steps, slow 1: Big steps, fast
				Bit[5]: Banding filter selection 0: OFF 1: ON, set minimum exposure to 1/120s
				Bit[4]: Auto banding filter 0: Banding filter is always ON/OFF depending on AUTO_1[5] (R0x3013[5]) setting 1: Automatically disable the banding filter under strong light condition
				Bit[3]: Extreme bright exposure control enable 0: OFF, Tline <= Tex min. 1: ON, enable minimum exposure Tex min. ≤ Tline
				Bit[2]: Auto gain control auto/manual mode selection 0: Manual 1: Auto
				Bit[1]: Not used
				Bit[0]: Auto exposure control auto/manual mode selection 0: Manual 1: Auto

table 7-1 system control registers (sheet 4 of 9)

address	register name	default value	R/W	description
0x3014	AUTO_2[7:0]	0x04	RW	Auto Control 2
				Bit[7]: Manually assign banding 0: 60Hz 1: 50Hz
				Bit[6]: Auto banding detection enable 0: Banding according to AUTO_2[7] (R0x3014[7]) manual setting 1: Banding depending on auto 50/60 Hz detection result
				Bit[5]: Reserved
				Bit[4]: Freeze AEC/AGC
				Bit[3]: Night mode enable 0: Disable 1: Enable
				Bit[2]: BDcAEC - enable banding AEC smooth switch between 50/60
				Bit[1]: Manually assign extreme bright exposure enable 0: Auto exposure 1: Exposure based on AECL[7:0] (R0x3014[7:0]) steps
				Bit[0]: Banding filter option 0: Disable 1: Enable
0x3015	AUTO_3[7:0]	0x02	RW	Auto Control 3
				Bit[7]: Not used
				Bit[6:4]: Dummy frame control 000: No dummy frame 001: Allow 1 dummy frame 010: Allow 2 dummy frames 011: Allow 3 dummy frames 100: Allow 7 dummy frames
				Bit[3]: Not used
				Bit[2:0]: AGC gain ceiling, GH[2:0]: 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x 101: 64x 110: 128x 111: 128x

table 7-1 system control registers (sheet 5 of 9)

address	register name	default value	R/W	description
0x3018	WPT/HISH[7:0]	0x78	RW	Luminance Signal/Histogram High Range for AEC/AGC operation Shared by average and histogram based algorithm AEC/AGC value decreases in auto mode when average luminance/histogram is greater than WPT/HisH[7:0]
0x3019	BPT/HISL[7:0]	0x68	RW	Luminance Signal/Histogram Low Range for AEC/AGC operation Shared by average and histogram based algorithm AEC/AGC value increases in auto mode when average luminance/histogram is less than BPT/HisL[7:0]
0x301A	VPT[7:0]	0xD4	RW	Fast Mode Large Step Range Thresholds - effective only in AEC/AGC fast mode Bit[7:4]: High threshold Bit[3:0]: Low threshold AEC/AGC may change in larger steps when luminance average is greater than VV[7:4] or less than VV[3:0]
0x301B	YAVG	0x00	RW	Luminance Average - this register will auto update Average luminance is calculated from the B/Gb/Gr/R channel average as follows: $B/Gb/Gr/R \text{ channel average} = (BAVG[7:0] + GbAVG[7:0] + GrAVG[7:0] + RAVG[7:0]) \times 0.25$
0x301C	AECG_MAX50	0x05	RW	50 Hz Smooth Banding Maximum Steps Control Bit[7:6]: Reserved Bit[5:0]: AECG_MAX50[5:0] 50 Hz smooth banding maximum steps
0x301D	AECG_MAX60	0x07	RW	60 Hz Smooth Banding Maximum Steps Control Bit[7:6]: Reserved Bit[5:0]: AECG_MAX60[5:0] 60 Hz smooth banding maximum steps
0x3020	HS[15:8]	0x01	RW	Horizontal Window Start 8 MSBs HS[15:0]: Horizontal start point of array, each bit represents 1 pixel

table 7-1 system control registers (sheet 6 of 9)

address	register name	default value	R/W	description
0x3021	HS[7:0]	0x0D	RW	Horizontal Window Start 8 LSBs HS[15:0]: Horizontal start point of array, each bit represents 1 pixel
0x3022	VS[15:8]	0x00	RW	Vertical Window Start 8 MSBs VS[15:0]: Vertical start point of array, each bit represents 1 scan line
0x3023	VS[7:0]	0x0A	RW	Vertical Window Start 8 LSBs VS[15:0]: Vertical start point of array, each bit represents 1 scan line
0x3024	HW[15:8]	0x18	RW	Horizontal Width 8 MSBs HW[15:0]: Output raw image pixels are from HS[15:0] to HS[15:0] + HW[15:0]
0x3025	HW[7:0]	0x00	RW	Horizontal Width 8 LSBs HW[15:0]: Output raw image pixels are from HS[15:0] to HS[15:0] + HW[15:0]
0x3026	VH[15:8]	0x06	RW	Vertical Height 8 MSBs VH[15:0]: Output raw image pixels are from VS[15:0] to VS[15:0] + VH[15:0]
0x3027	VH[7:0]	0x0C	RW	Vertical Height 8 LSBs VH[15:0]: Output raw image pixels are from VS[15:0] to VS[15:0] + VH[15:0]
0x3028	HTS[15:8]	0x09	RW	Horizontal Total Size 8 MSBs HTS[15:0]: Horizontal total size for 1 line
0x3029	HTS[7:0]	0x47	RW	Horizontal Total Size 8 LSBs HTS[15:0]: Horizontal total size for 1 line
0x302A	VTS[15:8]	0x06	RW	Vertical Total Size 8 MSBs VTS[15:0]: Vertical total size for 1 frame
0x302B	VTS[7:0]	0x20	RW	Vertical Total Size 9 LSBs VTS[15:0]: Vertical total size for 1 frame
0x302D	EXVTS[15:8]	0x00	RW	VSYSN Pulse Width 8 MSBs EXVTS[15:0]: Line periods added to VSYSN width. Default VSYSN output width is 4 × tline. Each LSB count will add 1 × Tline to the VSYSN active period.

table 7-1 system control registers (sheet 7 of 9)

address	register name	default value	R/W	description
0x302E	EXVTS[7:0]	0x00	RW	VSYNC Pulse Width LSB 8 bits EXVTS[15:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 × tline. Each LSB count will add 1 × Tline to the VSYNC active period.
0x3070	BD50[15:8]	0x00	RW	50Hz Banding 8 MSBs $50\text{Hz} = 1 / (\text{BD50}[15:0] \times \text{Tline})$
0x3071	BD50[7:0]	0xEB	RW	50Hz Banding 8 LSBs $50\text{Hz} = 1 / (\text{BD50}[15:0] \times \text{Tline})$
0x3072	BD60[15:8]	0x00	RW	60Hz Banding 8 MSBs $60\text{Hz} = 1 / (\text{BD60}[15:0] \times \text{Tline})$
0x3073	BD60[7:0]	0xC4	RW	60Hz Banding 8 LSBs $60\text{Hz} = 1 / (\text{BD60}[15:0] \times \text{Tline})$
0x3077	TMC1	0x00	RW	Timing Control 1 Bit[7]: CHSYNC pin output swap 0: CHSYNC 1: HREF Bit[6]: HREF pin output swap 0: HREF 1: CHSYNC Bit[5:4]: Reserved Bit[3]: HREF output polarity 0: Output positive HREF 1: Output negative HREF, HREF negative for data valid Bit[2]: Reserved Bit[1]: VSYNC polarity 0: Positive 1: Negative Bit[0]: HSYNC polarity 0: Positive 1: Negative
0x307A	TMC4	0x00	RW	Timing Control 4 Bit[7:0]: RSTRB[7:0] - flash light control
0x307B	TMC5	0x40	RW	Timing Control 5 Bit[7:4]: Reserved Bit[3]: Digital color bar enable Bit[2:0]: Pattern - select digital color bar pattern

table 7-1 system control registers (sheet 8 of 9)

address	register name	default value	R/W	description
0x307C	TMC6	0x00	RW	Timing Control 6 Bit[7:2]: Reserved Bit[1]: Horizontal mirror Bit[0]: Vertical flip
0x307D	TMC7	0x00	RW	Timing Control 7 Bit[7]: Color bar test pattern 0: OFF 1: ON Bit[6:0]: Reserved
0x3080	TMCA	0x11	RW	Timing Control A Bit[7]: Output pattern option Bit[6:0]: Reserved
0x3081	TMCB	0x04	RW	Timing Control B Bit[7]: MIRROR_OPT - pixel shift while mirroring 0: OFF 1: ON Bit[6]: OTP memory clock option 0: Slow 1: Fast Bit[5:1]: Reserved Bit[0]: Swap MSB and LSB at the output port
0x3086	TMC10	0x00	RW	Timing Control 10 Bit[7:4]: Reserved Bit[3]: Sys_reset, Sys_rest_pll Enable Bit[2]: RegSleep option Bit[1]: Sleep option Bit[0]: Sleep ON/OFF 0: OFF 1: ON
0x3088	ISP_XOUT[15:8]	0x80	RW	ISP X-direction Output Size [15:8] Bit[7:4]: Not used Bit[3:0]: X_size_in[11:8]
0x3089	ISP_XOUT[7:0]	0x00	RW	ISP X-direction Output Size [7:0]
0x308A	ISP_YOUT[15:8]	0x06	RW	ISP Y-direction Output Size [15:8] Bit[7:3]: Not used Bit[2:0]: X_size_in[10:8]
0x308B	ISP_YOUT[7:0]	0x00	RW	ISP Y-direction Output Size [7:0]
0x308C	RSVD	—	—	Reserved

table 7-1 system control registers (sheet 9 of 9)

address	register name	default value	R/W	description
0x308D	TMC13	0x00	RW	Timing Control 13 Bit[7]: RegSleep setting Bit[6:2]: Reserved Bit[1]: RegSleep option Bit[0]: Reserved
0x308F	OTP	–	R	OTP Memory Internal Registers Data Readout
0x3090~0x30AF	RSVD	–	–	Reserved
0x30B0	IO_CTRL0	0xFF	RW	IO Control 0 CY[7:0]
0x30B1	IO_CTRL1	0xEF	RW	IO Control 1 C_GP[1:0], C_VSYNC, C_STROBE, C_PCLK, C_HREF, CY[9:8]
0x30B2	IO_CTRL2	0x00	RW	IO Control 2 GPO_monitor, C_FREX, R_PAD[3:0]
0x30B3	RSVD	–	–	Reserved
0x30B4	DVP0	0x00	RW	GPO[3:0]

table 7-2 FMT_MUX registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3400	FMT_MUX_CTRL0	0x04	RW	Bit[7:3]: Reserved Bit[2:0]: Fmt_sel 000: ISP YUV 001: ISP RGB 010: ISP YUV422 011: ISP RAW 100: Int CIF RAW 101: Ext CIF RAW 110: Ext CIF YUV422 bypass
0x3401~0x3402	RSVD	–	–	Reserved
0x3403	ISP_PAD_CTR2	0x00	RW	Bit[7:4]: X start Bit[3:0]: Y start

table 7-2 FMT_MUX registers (sheet 2 of 3)

address	register name	default value	R/W	description
				Bit[7] UV_sel 0: Use UV_avg, Y 1: Use U0Y0, V0Y1 Bit[6]: YUV422_in 0: Input to FORMAT is raw data 1: Input to FORMAT is YUV422 data when bypassing FORMAT Bit[5:0]: YUV422: 0x00: yuyvyuyv.../yuyvyuyv... 0x01: yvyuyvyu.../yvyuyvyu... 0x02: uyvyuyvy.../uyvyuyvy... 0x03: vyuyvyuy.../vyuyvyuy... YUV420: 0x04: yyyy.../yuyvyuyv... 0x05: yyyy.../yvyuyvyu... 0x06: yyyy.../uyvyuyvy... 0x07: yyyy.../vyuyvyuy... 0x08: yuyvyuyv.../yyyy... 0x09: yvyuyvyu.../yyyy... 0x0A: uyvyuyvy.../yyyy... 0x0B: vyuyvyuy.../yyyy... 0x0C: uyyuyy.../vyvyvy Y8: 0x0D: yyyy.../yyyy... YUV444(RGB888): 0x0E: yuyvuv.../yuyvuv... (gbrgrb.../gbrgrb...) 0x0F: yvuyvu.../yvuyvu... (grbgrb.../grbgrb...) 0x1C: uyvyuyv.../uyvyuyv... (bgrbgr.../bgrbgr...) 0x1D: vyuyvu.../vyuyvu... (rgbrgb.../rgbrgb...) 0x1E: uyvyuyv.../uyvyuyv... (brgbrg.../brgbrg...) 0x1F: vuyvuy.../vuyvuy... (rbgrbg.../rbgrbg...) RGB565: 0x10: {b[4:0],g[5:3]}, {g[2:0],r[4:0]} 0x11: {r[4:0],g[5:3]}, {g[2:0],b[4:0]} 0x30: {g[2:0],b[4:0]}, {r[4:0],g[5:3]} (MIPI RGB565)
0x3404	FMT_CTRL00	0x02	RW	

table 7-2 FMT_MUX registers (sheet 3 of 3)

address	register name	default value	R/W	description
				RGB555: 0x12: {b[4:0],g[4:2]}, {g[1:0],1'b0,r[4:0]} 0x13: {r[4:0],g[4:2]}, {g[1:0],1'b0,b[4:0]} 0x32: {g[1:0],1'b0,b[4:0]}, {r[4:0],g[4:2]} (MIPI RGB555) RGB444: 0x14: {b[3:0],1'b0,g[3:1]}, {g[0],2'h0,r[3:0],1'b0} 0x15: {r[3:0],1'b0,g[3:1]}, {g[0],2'h0,b[3:0],1'b0} 0x34: {g[0],2'h0,b[3:0],1'b0}, {r[3:0],1'b0,g[3:1]} (MIPI RGB444) 0x37: {4'b0,r[3:0]}, {g[3:0],b[3:0]} 0x38: {4'b0,b[3:0]}, {g[3:0],r[3:0]} 0x16: {b[3:0],g[3:0]}, {r[3:0],b[3:0]} ... 0x17: {r[3:0],g[3:0]}, {b[3:0],r[3:0]} ... Raw: 0x18: bgbg..../grgr.... 0x19: gbgb..../rgrg.... 0x1A: grgr..../bgbg.... 0x1B: rrgg..../gbgb....
0x3405	DITHER_CTRL0	0x40	RW	Bit[7]: Reserved Bit[6]: Dither_sel 0: Use register seting 1: Follow with fmt_control Bit[5:4]: R_dithering 00: No 01: 4-bit 10: 5-bit 11: 6-bit Bit[3:2]: G_dithering 00: No 01: 4-bit 10: 5-bit 11: 6-bit Bit[1:0]: B_dithering 00: No 01: 4-bit 10: 5-bit 11: 6-bit

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8 electrical specifications

table 8-1 absolute maximum ratings

parameter		absolute maximum rating ^a
stable operating temperature		0°C to +50°C
operating temperature		-20°C to +70°C
ambient storage temperature		-40°C to +95°C
ambient humidity		TBD
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-C}	3V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to $V_{DD-IO} + 1V$
lead-free temperature, surface-mount process		245°C

- a. Exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device.

table 8-2 DC characteristics ($-20^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$)

symbol	parameter	min	typ	max	unit
supply					
V _{DD-A}	supply voltage (analog)	2.5	2.8	3.0	V
V _{DD-D}	supply voltage (digital core)	1.425	1.5	1.575	V
V _{DD-IO}	supply voltage (digital I/O)	1.71	1.8	3.0	V
I _{DD-A}	active (operating) current	TBD	TBD	TBD	mA
I _{DD-D}		TBD	TBD	TBD	mA
I _{DD-IO}		TBD	TBD	TBD	mA
I _{DDS-SCCB}	standby current	TBD	TBD	TBD	mA
I _{DDS-PWDN}		TBD	TBD	TBD	μA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.5V, DOVDD = 1.8V)					
V _{IL}	input voltage LOW			0.54	V
V _{IH}	input voltage HIGH	1.26			V
C _{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V _{OH}	output voltage HIGH	1.62			V
V _{OL}	output voltage LOW			0.18	V
serial interface inputs					
V _{IL} ^a	SCL and SDA	-0.5	0	0.54	V
V _{IH} ^a	SCL and SDA	1.26	1.8	2.3	V

a. Based on DOVDD = 1.8V.

table 8-3 AC characteristics ($T_A = 25^\circ\text{C}$, $V_{DD-A} = 2.8\text{V}$)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth		30		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	setting time for hardware reset			<1	ms
	setting time for software reset			<1	ms
	setting time for UXGA/SVGA mode change			<1	ms
	setting time for register setting			<300	ms
digital inputs					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}	SCL and SDA	-0.5	0	0.54	V
V_{IH}	SCL and SDA	1.26	1.8	2.3	V

table 8-4 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{osc}	frequency (XVCLK)	6	24	27	MHz
t_r, t_f	clock input rise/fall time			5 (10 ^a)	ns

a. if using the internal PLL

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9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications

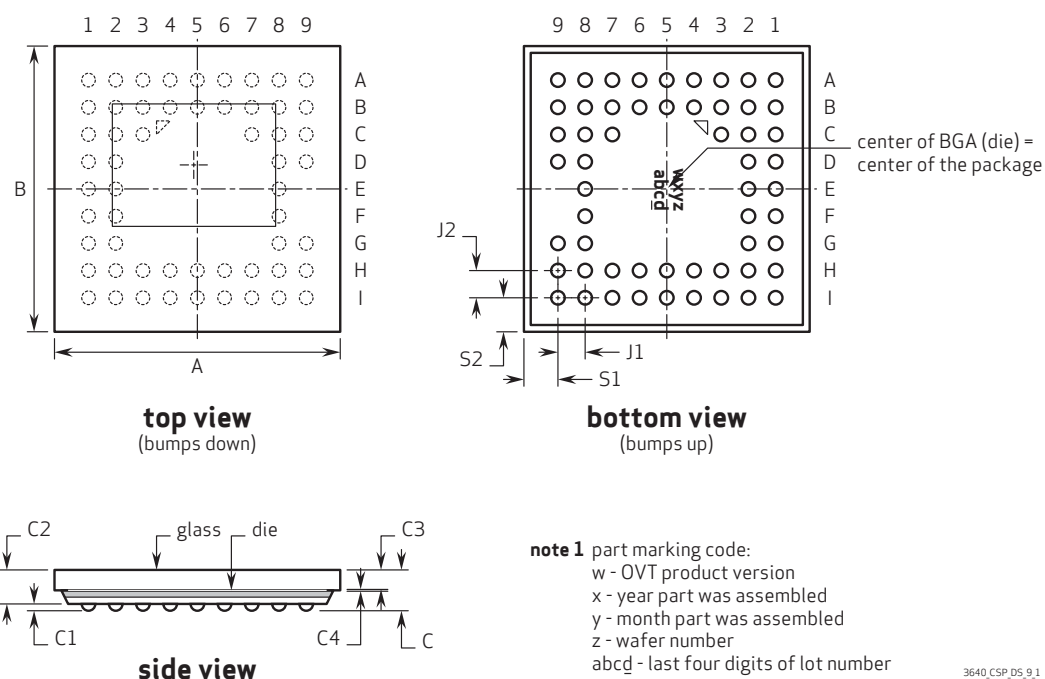


table 9-1 package dimensions (sheet 1 of 2)

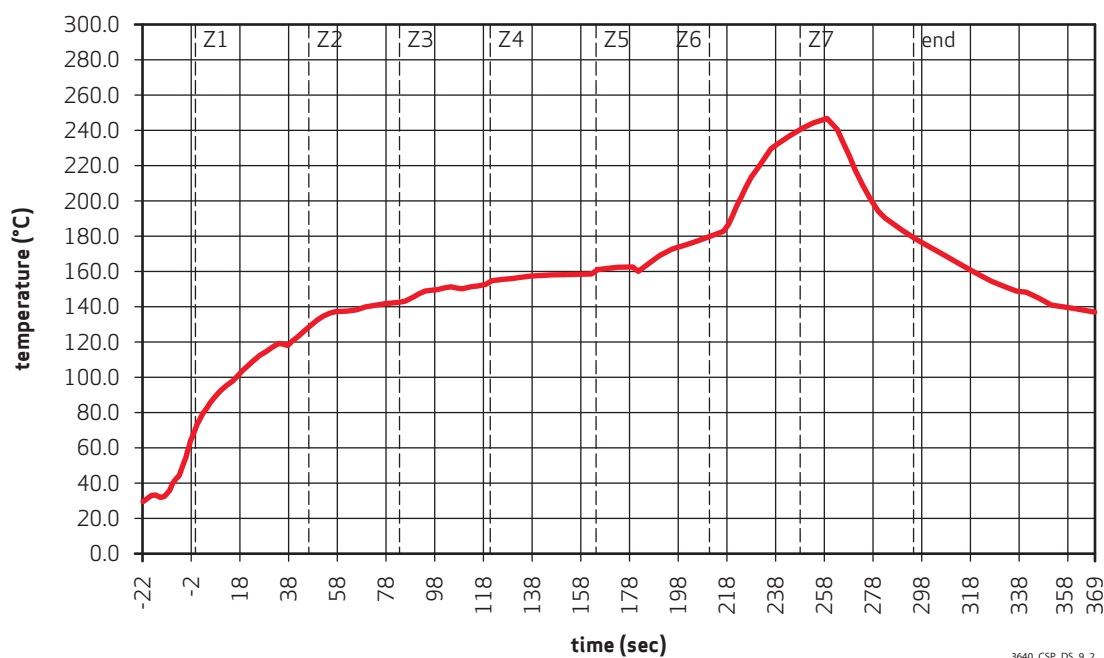
parameter	symbol	min	typ	max	unit
package body dimension x	A	6260	6285	6310	μm
package body dimension y	B	6100	6125	6150	μm
package height	C	825	885	945	μm
ball height	C1	130	160	190	μm
package body thickness	C2	680	725	770	μm
cover glass thickness	C3	375	400	425	μm
airgap between cover glass and sensor	C4	30	45	60	μm
ball diameter	D	270	300	330	μm

table 9-1 package dimensions (sheet 2 of 2)

parameter	symbol	min	typ	max	unit
total pin count	N		56 (11 NC)		
pin count x-axis	N1		9		
pin count y-axis	N2		9		
pins pitch x-axis	J1		610		μm
pins pitch y-axis	J2		610		μm
edge-to-pin center distance analog x	S1	673	703	733	μm
edge-to-pin center distance analog y	S2	593	623	653	μm

9.2 IR reflow specifications

figure 9-2 IR reflow ramp rate requirements



note

The OV3640 uses a lead free package.

table 9-2 reflow conditions

condition	exposure
average ramp-up rate (30°C to 217°C)	less than 3°C per second
> 100°C	between 330 - 600 seconds
> 150°C	at least 210 seconds
> 217°C	at least 30 seconds (30 ~ 120 seconds)
peak temperature	245°C
cool-down rate (peak to 50°C)	less than 6°C per second
time from 30°C to 245°C	no greater than 390 seconds

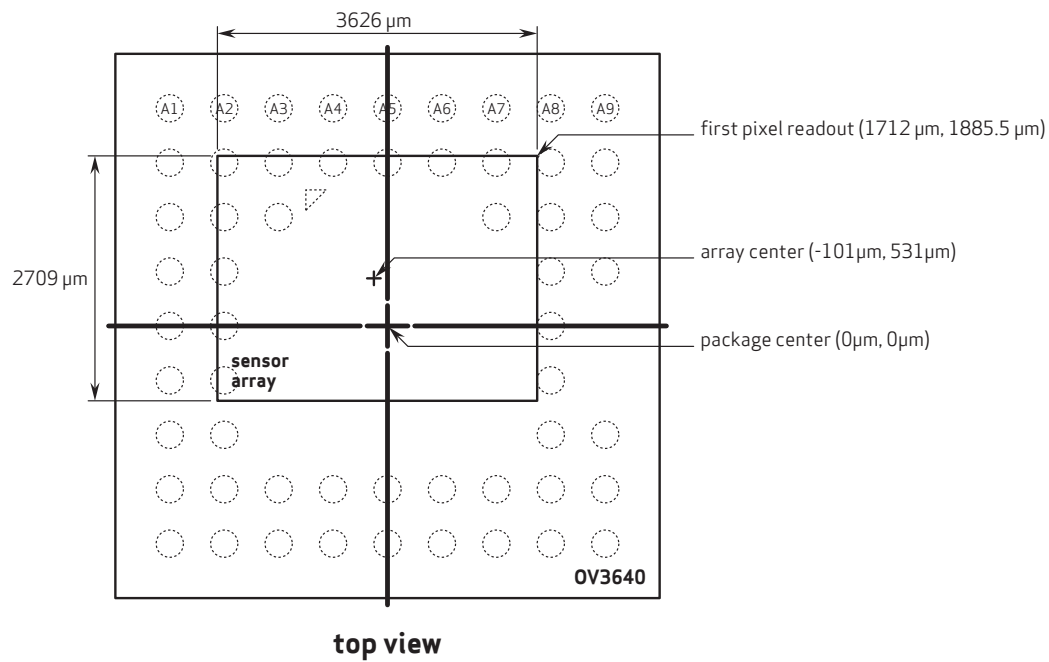
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10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A9 oriented down on the PCB.

3640_CSP_DS_10_1

10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)

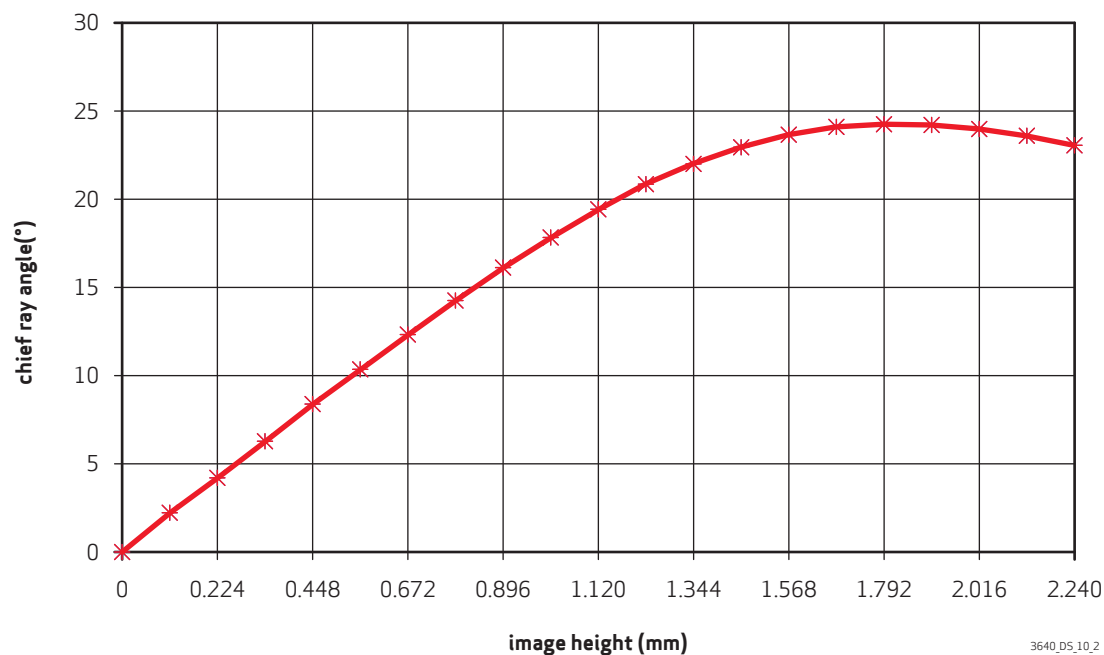


table 10-1 CRA versus image height plot (sheet 1 of 2)

field (%)	image height (mm)	CRA (degrees)
0	0	0
0.05	0.112	2.18
0.1	0.224	4.2
0.15	0.336	6.28
0.2	0.448	8.34
0.25	0.56	10.36
0.3	0.672	12.35
0.35	0.784	14.28
0.4	0.896	16.13
0.45	1.008	17.86

table 10-1 CRA versus image height plot (sheet 2 of 2)

field (%)	image height (mm)	CRA (degrees)
0.5	1.12	19.45
0.55	1.232	20.85
0.6	1.344	22.03
0.65	1.456	22.98
0.7	1.568	23.67
0.75	1.68	24.11
0.8	1.792	24.29
0.85	1.904	24.24
0.9	2.016	23.99
0.95	2.128	23.6
1	2.24	23.07

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