ST77922

Single-Chip TFT Controller/Driver/Touch

Datasheet

Preliminarily 0.1

2023/06

Sitronix Technology Corporation

LIST OF CONTENT

1 GENERAL DESCRIPTION

The ST77922 is a System-on-Chip (SoC) driver LSI designed for TFT LCD controller with a build-in touch panel controller and suitable for small to medium size portable devices. ST77922 can support up to 160,000 pixels in resolution with RAM for dual gate, 560RGBx640 Ram-less for dual gate and support 16,777,216-color. The 840-channel source driver has true 6-bit resolution, which generates 64 Gamma-corrected values by an internal D/A converter. The ST77922 is capable of connecting directly to an external microprocessor, and provides 8-bits parallel interface, 8-bit RGB Interface, MIPI interface, 3/4-line serial peripheral interface (3/4 SPI), and Quad serial peripheral interface (QSPI). The ST77922 touch protocol via standard integrated circuit bus(I2C) or serial peripheral interface(SPI). Display data can be stored in the on-chip display data RAM . It can perform display data RAM read/write operation with no external operation clock to minimize power consumption. In addition, because of the integrated power supply circuit necessary to drive liquid crystal; it is possible to make a display system with fewest components.

2 FEATURES

2.1 Display

- Single chip TFT-LCD Controller/Driver with On-chip Display 1/2RAM(200x400*24bits)
- Display Resolution: Dual Gate
  - 400*RGB (H) *400(V) ~ 120*RGB (H) *120(V)
  - 400RGB~560*RGB (H) *640(V) , Ram-less
- LCD Driver Output Circuits
  - Source Outputs: 280 RGB Channels
  - Support gate control signals to gate driver in the panel
- Display Colors (Color Mode)
  - Full Color: 16.7M, RGB=(888) max., Idle Mode Off
  - Color Reduce: 8-color, RGB=(111), Idle Mode On
- Programmable Pixel Color Format (Color Depth) for Various Display Data Input Format
  - 16-bit/pixel: RGB=(565) 65K color
  - 18-bit/pixel: RGB=(666) 262K color
  - 24-bit/pixel: RGB=(888) 16.7M color
- Interface
  - Parallel 8080-series MCU Interface (8-bit)
  - 8-bit RGB Interface (VSYNCX, HSYNCX, DOTCLK, ENABLE, DB[7:0])
  - Serial Peripheral Interface (SPI Interface) and 2 data lane SPI
  - Quad Serial Peripheral Interface (QSPI Interface)
  - MIPI Display Serial Interface (DSI V1.01 r11 and D-PHY V1.0, 1 clock and 1 data lane pairs)
- Display Features
  - CDC Function
  - CABC Function
  - Sunlight Readability Enhancement (SRE)
- On Chip Build-In Circuits
  - DC/DC Converter
  - Non-Volatile (NV) Memory
  - Adjustable VCOM Generation
  - Timing Controller
  - Internal VPP for NV Memory
- Build-In NV Memory for LCD Initial Register Setting
  - OTP to store ID1~ID3
  - OTP to store VCOM/VCC/VREGP/VREGN calibration
  - OTP to store CDC and Factory Default Value (Module ID, Module Version, and etc.)
  - OTP to store panel timing, analog power setting, and etc.

- Driving Algorithm
  - 1/2/4-dot Inversion
  - Column Inversion
- Wide Supply Voltage Range
  - I/O Voltage (VDDI to GND): 1.65V ~ 3.3V (VDDI≦VDD)
  - Voltage for Analog Circuit (VDD to GND): 2.65V ~ 3.3V
- On-Chip Power System
  - VCOM level: GND
  - Gamma(+) voltage range: 3.8V~6.4V
  - Gamma(-) voltage range: -4.4V~-2V
  - VGH voltage range: 7.5V~15.5V
  - VGL voltage range: -6.5V~-12V
  - Adjustable voltage range for feed through compensation: 0.1V~2.2V
- Power saving modes
  - Sleep in mode
  - Deep Standby mode
  - Low frame mode 1~50Hz
- Others
  - Zero-Cap
  - GIP + Dual-Gate driving
  - Zigzag Panel
  - Dual-Gate: pixel number must be a multiple of 4
- Optimized layout for COG Assembly
- Operate temperature range: −30ºC to +85 ºC
- Lower Power Consumption

2.2 Touch

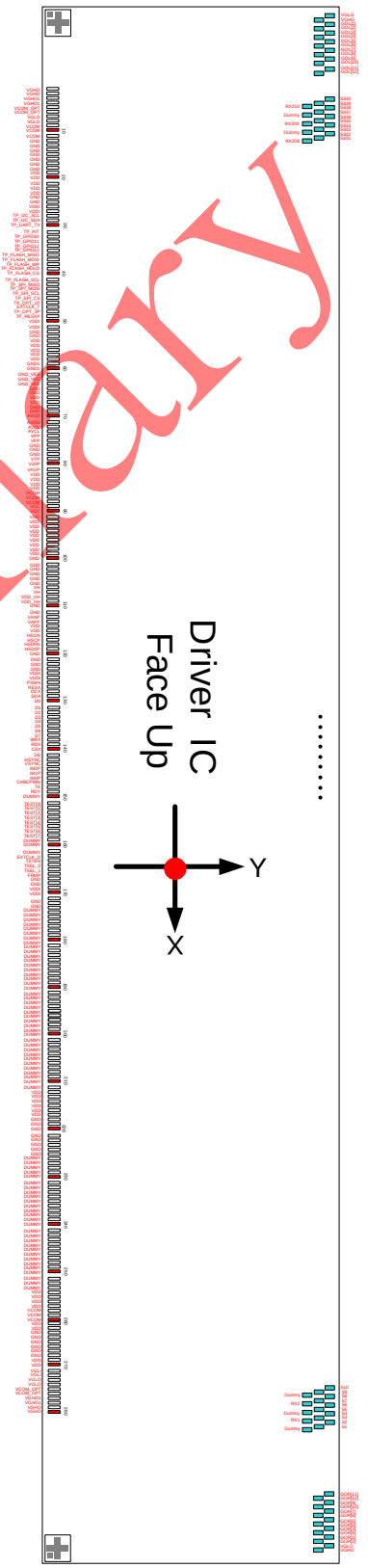
- 16-bits MCU optimized for capacitive sensing and other human interactions

- 5-point coordinate sensing without ghost point
- 210 RX Channel
- TP Sensor Pitch : 4mm x 4mm or more
- High signal to noise ratio(SNR)
- I2C & SPI protocol for communication with the host
- Support Long-V sensing mode
- Support noise detection and automatic frequency hopping
- Support Flush function
- Wake Up gesture
- Self-Capacitance detection
- Power saving for Finger Detection
- Touch mapping flexible
- Touch interface access Display register
- Touch FW Host/Flash download

3 PAD ARRANGEMENT

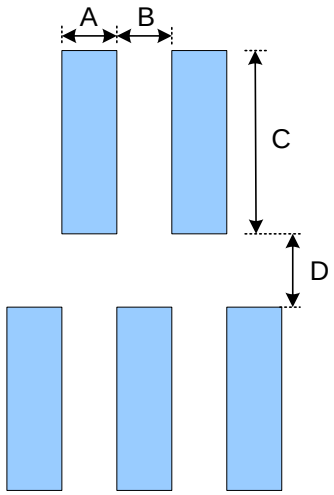
3.1 Output Bump Dimension

Au bump height	9um
Au bump size	**13μm x 70μm :** GIP : VGHO、VGL、GOR1~GOR12、GOL1~GOL12 Source : S1~S840 RX1~210
	30μm x 73μm : Pad1~Pad280



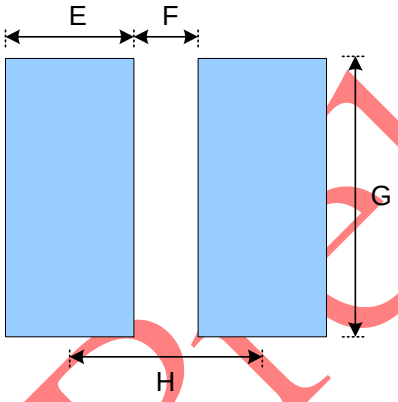
3.2 Bump Dimension

●Output Pads



Symbol	Item	Size
A	Bump Width	13 um
B	Bump Gap 1 (Horizontal)	15 um
C	Bump Height	70 um
D	Bump Gap 2 (Vertical)	20 um

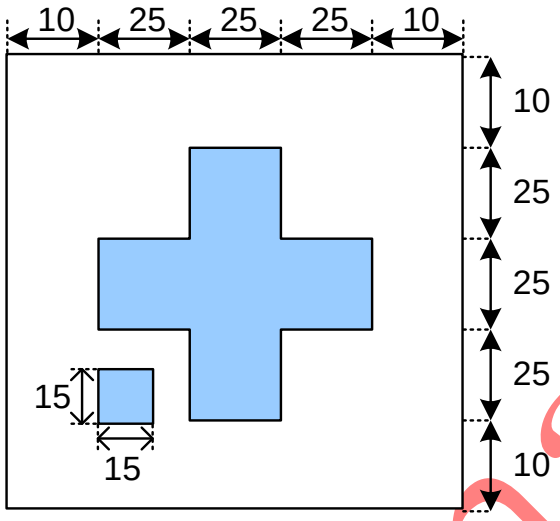
●Input Pads



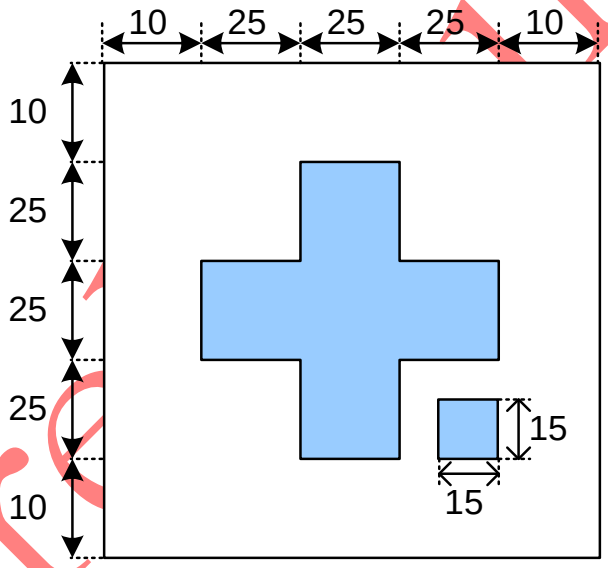
Symbol	Item	Size
E	Bump Width	30 um
F	Bump Gap	15 um
G	Bump Height	73 um
H	Bump Pitch	45 or 49 um

3.3 Alignment Mark Dimension

● **Alignment Mark Left: L(X,Y)=(-6676.8, -431.954)**



● **Alignment Mark Right: R(X,Y)= (6677.201, -431.954)**



3.4 Chip Information

Chip size	13460 um x 970 um
Chip thickness	200 um
Pad Location	Pad center
Coordinate Origin	Chip center

Note: The chip size is not include the scribe line.u

4 PAD ARRANGEMENT

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	VGHO	-6257	-439.5	34	TP_GPIO12	-4748	-439.5
2	VGHO	-6212	-439.5	35	TP_GPIO13	-4699	-439.5
3	VGHO1	-6167	-439.5	36	TP_FLASH_MISO	-4650	-439.5
4	VGHO1	-6122	-439.5	37	TP_FLASH_MOSI	-4605	-439.5
5	VCOM_OPT	-6077	-439.5	38	TP_FLASH_WP	-4560	-439.5
6	VCOM_OPT	-6032	-439.5	39	TP_FLASH_HOLD	-4515	-439.5
7	VGLO	-5987	-439.5	40	TP_FLASH_CS	-4470	-439.5
8	VGLO	-5942	-439.5	41	TP_FLASH_SCL	-4425	-439.5
9	VCOM	-5897	-439.5	42	TP_SPI_MISO	-4380	-439.5
10	VCOM	-5852	-439.5	43	TP_SPI_MOSI	-4335	-439.5
11	VCOM	-5807	-439.5	44	TP_SPI_SCL	-4290	-439.5
12	GND	-5762	-439.5	45	TP_SPI_CS	-4245	-439.5
13	GND	-5717	-439.5	46	TP_OPT_1P	-4200	-439.5
14	GND	-5672	-439.5	47	EXTCLK_T	-4155	-439.5
15	GND	-5627	-439.5	48	TP_OPT_3P	-4110	-439.5
16	GND	-5582	-439.5	49	TP_RESXP	-4065	-439.5
17	GND	-5537	-439.5	50	VDDI	-4020	-439.5
18	GND	-5492	-439.5	51	VDDI	-3975	-439.5
19	VDD	-5447	-439.5	52	GND	-3930	-439.5
20	VDD	-5402	-439.5	53	GND	-3885	-439.5
21	VDD	-5357	-439.5	54	VDD	-3840	-439.5
22	VDD	-5312	-439.5	55	VDD	-3795	-439.5
23	VDD	-5267	-439.5	56	VDD	-3750	-439.5
24	GND	-5222	-439.5	57	VDD	-3705	-439.5
25	GND	-5177	-439.5	58	VDD	-3660	-439.5
26	VDDI	-5132	-439.5	59	GND1	-3615	-439.5
27	VDDI	-5087	-439.5	60	GND1	-3570	-439.5
28	TP_I2C_SCL	-5042	-439.5	61	GND_VEE	-3525	-439.5
29	TP_I2C_SDA	-4993	-439.5	62	GND_VEE	-3480	-439.5
30	TP_UART_TX	-4944	-439.5	63	GND_VEE	-3435	-439.5
31	TP_INT	-4895	-439.5	64	GND	-3390	-439.5
32	TP_GPIO10	-4846	-439.5	65	GND	-3345	-439.5
33	TP_GPIO11	-4797	-439.5	66	VDD	-3300	-439.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
67	VDD	-3255	-439.5	101	GND	-1725	-439.5
68	GND	-3210	-439.5	102	GND	-1680	-439.5
69	GND	-3165	-439.5	103	GND	-1635	-439.5
70	AVDD	-3120	-439.5	104	GND	-1590	-439.5
71	AVDD	-3075	-439.5	105	GND	-1545	-439.5
72	AVCL	-3030	-439.5	106	VH	-1500	-439.5
73	AVCL	-2985	-439.5	107	VH	-1455	-439.5
74	VPP	-2940	-439.5	108	VDD_VH	-1410	-439.5
75	VPP	-2895	-439.5	109	VDD_VH	-1365	-439.5
76	GND	-2850	-439.5	110	GND	-1320	-439.5
77	GND	-2805	-439.5	111	GND	-1275	-439.5
78	GND	-2760	-439.5	112	VANP	-1230	-439.5
79	VTP	-2715	-439.5	113	VAPP	-1185	-439.5
80	V20P	-2670	-439.5	114	VDD	-1140	-439.5
81	VAGP	-2625	-439.5	115	VDD	-1095.96	-439.5
82	VDD	-2580	-439.5	116	HSCN	-1050	-439.5
83	VDD	-2535	-439.5	117	HSCP	-1005	-439.5
84	VDD	-2490	-439.5	118	HSD0N	-960	-439.5
85	VDD	-2445	-439.5	119	HSD0P	-915	-439.5
86	VCOM	-2400	-439.5	120	GND	-870	-439.5
87	VCOM	-2355	-439.5	121	GND	-825	-439.5
88	VCOM	-2310	-439.5	122	GND	-780	-439.5
89	VCC	-2265	-439.5	123	GND	-735	-439.5
90	VCC	-2220	-439.5	124	VDDI	-690	-439.5
91	VDD	-2175	-439.5	125	VDDI	-645	-439.5
92	VDD	-2130	-439.5	126	PSWA	-600	-439.5
93	VDD	-2085	-439.5	127	RESX	-555	-439.5
94	VDD	-2040	-439.5	128	DCX	-506	-439.5
95	VDD	-1995	-439.5	129	SDA	-457	-439.5
96	VDD	-1950	-439.5	130	D0	-408	-439.5
97	VDD	-1905	-439.5	131	D1	-359	-439.5
98	VDD	-1860	-439.5	132	D2	-310	-439.5
99	VDD	-1815	-439.5	133	D3	-261	-439.5
100	GND	-1770	-439.5	134	D4	-212	-439.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
135	D5	-163	-439.5	169	VDDI	1375	-439.5
136	D6	-114	-439.5	170	VDDI	1420	-439.5
137	D7	-65	-439.5	171	GND	1465	-439.5
138	WRX	-20	-439.5	172	GND	1510	-439.5
139	RDX	25	-439.5	173	DUMMY	1555	-439.5
140	CSX	70	-439.5	174	DUMMY	1600	-439.5
141	DE	115	-439.5	175	DUMMY	1645	-439.5
142	HSYNC	160	-439.5	176	DUMMY	1690	-439.5
143	VSYNC	205	-439.5	177	DUMMY	1735	-439.5
144	IM2P	250	-439.5	178	DUMMY	1780	-439.5
145	IM1P	295	-439.5	179	DUMMY	1825	-439.5
146	IM0P	340	-439.5	180	DUMMY	1870	-439.5
147	CABCPWM	385	-439.5	181	DUMMY	1915	-439.5
148	TE	430	-439.5	182	DUMMY	1960	-439.5
149	RDY	475	-439.5	183	DUMMY	2005	-439.5
150	DUMMY	520	-439.5	184	DUMMY	2050	-439.5
151	TEST[0]	565	-439.5	185	DUMMY	2095	-439.5
152	TEST[1]	610	-439.5	186	DUMMY	2140	-439.5
153	TEST[2]	655	-439.5	187	DUMMY	2185	-439.5
154	TEST[3]	700	-439.5	188	DUMMY	2230	-439.5
155	TEST[4]	745	-439.5	189	DUMMY	2275	-439.5
156	TEST[5]	790	-439.5	190	DUMMY	2320	-439.5
157	TEST[6]	835	-439.5	191	DUMMY	2365	-439.5
158	TEST[7]	880	-439.5	192	DUMMY	2410	-439.5
159	DUMMY	925	-439.5	193	DUMMY	2455	-439.5
160	DUMMY	970	-439.5	194	DUMMY	2500	-439.5
161	DUMMY	1015	-439.5	195	DUMMY	2545	-439.5
162	EXTCLK_D	1060	-439.5	196	DUMMY	2590	-439.5
163	TSTEN	1105	-439.5	197	DUMMY	2635	-439.5
164	TSEL_0	1150	-439.5	198	DUMMY	2680	-439.5
165	TSEL_1	1195	-439.5	199	DUMMY	2725	-439.5
166	FRMP	1240	-439.5	200	DUMMY	2770	-439.5
167	GND	1285	-439.5	201	DUMMY	2815	-439.5
168	GND	1330	-439.5	202	DUMMY	2860	-439.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
203	DUMMY	2905	-439.5	237	DUMMY	4435	-439.5
204	DUMMY	2950	-439.5	238	DUMMY	4480	-439.5
205	DUMMY	2995	-439.5	239	DUMMY	4525	-439.5
206	DUMMY	3040	-439.5	240	DUMMY	4570	-439.5
207	DUMMY	3085	-439.5	241	DUMMY	4615	-439.5
208	DUMMY	3130	-439.5	242	DUMMY	4660	-439.5
209	DUMMY	3175	-439.5	243	DUMMY	4705	-439.5
210	DUMMY	3220	-439.5	244	DUMMY	4750	-439.5
211	DUMMY	3265	-439.5	245	DUMMY	4795	-439.5
212	VDD	3310	-439.5	246	DUMMY	4840	-439.5
213	VDD	3355	-439.5	247	DUMMY	4885	-439.5
214	VDD	3400	-439.5	248	DUMMY	4930	-439.5
215	VDD	3445	-439.5	249	DUMMY	4975	-439.5
216	VDD	3490	-439.5	250	DUMMY	5020	-439.5
217	VDD	3535	-439.5	251	DUMMY	5065	-439.5
218	GND	3580	-439.5	252	DUMMY	5110	-439.5
219	GND	3625	-439.5	253	DUMMY	5155	-439.5
220	GND	3670	-439.5	254	VDD	5200	-439.5
221	GND	3715	-439.5	255	VDD	5245	-439.5
222	GND	3760	-439.5	256	VDD	5290	-439.5
223	GND	3805	-439.5	257	VDD	5335	-439.5
224	GND	3850	-439.5	258	VCOM	5380	-439.5
225	GND	3895	-439.5	259	VCOM	5425	-439.5
226	DUMMY	3940	-439.5	260	VCOM	5470	-439.5
227	DUMMY	3985	-439.5	261	VDD	5515	-439.5
228	DUMMY	4030	-439.5	262	VDD	5560	-439.5
229	DUMMY	4075	-439.5	263	GND	5605	-439.5
230	DUMMY	4120	-439.5	264	GND	5650	-439.5
231	DUMMY	4165	-439.5	265	GND	5695	-439.5
232	DUMMY	4210	-439.5	266	GND	5740	-439.5
233	DUMMY	4255	-439.5	267	GND	5785	-439.5
234	DUMMY	4300	-439.5	268	GND	5830	-439.5
235	DUMMY	4345	-439.5	269	VDD	5875	-439.5
236	DUMMY	4390	-439.5	270	VDD	5920	-439.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
271	VGLI	5965	-439.5	305	S7	6295.15	325.945
272	VGLI	6010	-439.5	306	S8	6285.85	415.945
273	VGLO	6055	-439.5	307	DUMMY	6276.45	235.945
274	VGLO	6100	-439.5	308	S9	6267.15	325.945
275	VCOM_OPT	6145	-439.5	309	S10	6257.85	415.945
276	VCOM_OPT	6190	-439.5	310	RX3	6248.45	235.945
277	VGHO1	6235	-439.5	311	S11	6239.15	325.945
278	VGHO1	6280	-439.5	312	S12	6229.85	415.945
279	VGHO	6325	-439.5	313	DUMMY	6220.45	235.945
280	VGHO	6370	-439.5	314	S13	6211.15	325.945
281	VGHO	6712.35	325.945	315	S14	6201.85	415.945
282	VGLO	6698.35	415.945	316	RX4	6192.45	235.945
283	GOR[2]	6684.35	325.945	317	S15	6183.15	325.945
284	GOR[1]	6670.35	415.945	318	S16	6173.85	415.945
285	GOR[4]	6656.35	325.945	319	DUMMY	6164.45	235.945
286	GOR[3]	6642.35	415.945	320	S17	6155.15	325.945
287	GOR[6]	6628.35	325.945	321	S18	6145.85	415.945
288	GOR[5]	6614.35	415.945	322	RX5	6136.45	235.945
289	GOR[8]	6600.35	325.945	323	S19	6127.15	325.945
290	GOR[7]	6586.35	415.945	324	S20	6117.85	415.945
291	GOR[10]	6572.35	325.945	325	DUMMY	6108.45	235.945
292	GOR[9]	6558.35	415.945	326	S21	6099.15	325.945
293	GOR[12]	6544.35	325.945	327	S22	6089.85	415.945
294	GOR[11]	6530.35	415.945	328	RX6	6080.45	235.945
295	DUMMY	6388.45	235.945	329	S23	6071.15	325.945
296	S1	6379.15	325.945	330	S24	6061.85	415.945
297	S2	6369.85	415.945	331	DUMMY	6052.45	235.945
298	RX1	6360.45	235.945	332	S25	6043.15	325.945
299	S3	6351.15	325.945	333	S26	6033.85	415.945
300	S4	6341.85	415.945	334	RX7	6024.45	235.945
301	DUMMY	6332.45	235.945	335	S27	6015.15	325.945
302	S5	6323.15	325.945	336	S28	6005.85	415.945
303	S6	6313.85	415.945	337	DUMMY	5996.45	235.945
304	RX2	6304.45	235.945	338	S29	5987.15	325.945

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
339	S30	5977.85	415.945	373	DUMMY	5660.45	235.945
340	RX8	5968.45	235.945	374	S53	5651.15	325.945
341	S31	5959.15	325.945	375	S54	5641.85	415.945
342	S32	5949.85	415.945	376	RX14	5632.45	235.945
343	DUMMY	5940.45	235.945	377	S55	5623.15	325.945
344	S33	5931.15	325.945	378	S56	5613.85	415.945
345	S34	5921.85	415.945	379	DUMMY	5604.45	235.945
346	RX9	5912.45	235.945	380	S57	5595.15	325.945
347	S35	5903.15	325.945	381	S58	5585.85	415.945
348	S36	5893.85	415.945	382	RX15	5576.45	235.945
349	DUMMY	5884.45	235.945	383	S59	5567.15	325.945
350	S37	5875.15	325.945	384	S60	5557.85	415.945
351	S38	5865.85	415.945	385	DUMMY	5432.85	235.945
352	RX10	5856.45	235.945	386	S61	5423.55	325.945
353	S39	5847.15	325.945	387	S62	5414.25	415.945
354	S40	5837.85	415.945	388	RX16	5404.85	235.945
355	DUMMY	5828.45	235.945	389	S63	5395.55	325.945
356	S41	5819.15	325.945	390	S64	5386.25	415.945
357	S42	5809.85	415.945	391	DUMMY	5376.85	235.945
358	RX11	5800.45	235.945	392	S65	5367.55	325.945
359	S43	5791.15	325.945	393	S66	5358.25	415.945
360	S44	5781.85	415.945	394	RX17	5348.85	235.945
361	DUMMY	5772.45	235.945	395	S67	5339.55	325.945
362	S45	5763.15	325.945	396	S68	5330.25	415.945
363	S46	5753.85	415.945	397	DUMMY	5320.85	235.945
364	RX12	5744.45	235.945	398	S69	5311.55	325.945
365	S47	5735.15	325.945	399	S70	5302.25	415.945
366	S48	5725.85	415.945	400	RX18	5292.85	235.945
367	DUMMY	5716.45	235.945	401	S71	5283.55	325.945
368	S49	5707.15	325.945	402	S72	5274.25	415.945
369	S50	5697.85	415.945	403	DUMMY	5264.85	235.945
370	RX13	5688.45	235.945	404	S73	5255.55	325.945
371	S51	5679.15	325.945	405	S74	5246.25	415.945
372	S52	5669.85	415.945	406	RX19	5236.85	235.945

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
407	S75	5227.55	325.945	441	S98	4910.25	415.945
408	S76	5218.25	415.945	442	RX25	4900.85	235.945
409	DUMMY	5208.85	235.945	443	S99	4891.55	325.945
410	S77	5199.55	325.945	444	S100	4882.25	415.945
411	S78	5190.25	415.945	445	DUMMY	4872.85	235.945
412	RX20	5180.85	235.945	446	S101	4863.55	325.945
413	S79	5171.55	325.945	447	S102	4854.25	415.945
414	S80	5162.25	415.945	448	RX26	4844.85	235.945
415	DUMMY	5152.85	235.945	449	S103	4835.55	325.945
416	S81	5143.55	325.945	450	S104	4826.25	415.945
417	S82	5134.25	415.945	451	DUMMY	4816.85	235.945
418	RX21	5124.85	235.945	452	S105	4807.55	325.945
419	S83	5115.55	325.945	453	S106	4798.25	415.945
420	S84	5106.25	415.945	454	RX27	4788.85	235.945
421	DUMMY	5096.85	235.945	455	S107	4779.55	325.945
422	S85	5087.55	325.945	456	S108	4770.25	415.945
423	S86	5078.25	415.945	457	DUMMY	4760.85	235.945
424	RX22	5068.85	235.945	458	S109	4751.55	325.945
425	S87	5059.55	325.945	459	S110	4742.25	415.945
426	S88	5050.25	415.945	460	RX28	4732.85	235.945
427	DUMMY	5040.85	235.945	461	S111	4723.55	325.945
428	S89	5031.55	325.945	462	S112	4714.25	415.945
429	S90	5022.25	415.945	463	DUMMY	4704.85	235.945
430	RX23	5012.85	235.945	464	S113	4695.55	325.945
431	S91	5003.55	325.945	465	S114	4686.25	415.945
432	S92	4994.25	415.945	466	RX29	4676.85	235.945
433	DUMMY	4984.85	235.945	467	S115	4667.55	325.945
434	S93	4975.55	325.945	468	S116	4658.25	415.945
435	S94	4966.25	415.945	469	DUMMY	4648.85	235.945
436	RX24	4956.85	235.945	470	S117	4639.55	325.945
437	S95	4947.55	325.945	471	S118	4630.25	415.945
438	S96	4938.25	415.945	472	RX30	4620.85	235.945
439	DUMMY	4928.85	235.945	473	S119	4611.55	325.945
440	S97	4919.55	325.945	474	S120	4602.25	415.945

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
475	DUMMY	4592.85	235.945	509	S143	4275.55	325.945
476	S121	4583.55	325.945	510	S144	4266.25	415.945
477	S122	4574.25	415.945	511	DUMMY	4256.85	235.945
478	RX31	4564.85	235.945	512	S145	4247.55	325.945
479	S123	4555.55	325.945	513	S146	4238.25	415.945
480	S124	4546.25	415.945	514	RX37	4228.85	235.945
481	DUMMY	4536.85	235.945	515	S147	4219.55	325.945
482	S125	4527.55	325.945	516	S148	4210.25	415.945
483	S126	4518.25	415.945	517	DUMMY	4200.85	235.945
484	RX32	4508.85	235.945	518	S149	4191.55	325.945
485	S127	4499.55	325.945	519	S150	4182.25	415.945
486	S128	4490.25	415.945	520	RX38	4172.85	235.945
487	DUMMY	4480.85	235.945	521	S151	4163.55	325.945
488	S129	4471.55	325.945	522	S152	4154.25	415.945
489	S130	4462.25	415.945	523	DUMMY	4144.85	235.945
490	RX33	4452.85	235.945	524	S153	4135.55	325.945
491	S131	4443.55	325.945	525	S154	4126.25	415.945
492	S132	4434.25	415.945	526	RX39	4116.85	235.945
493	DUMMY	4424.85	235.945	527	S155	4107.55	325.945
494	S133	4415.55	325.945	528	S156	4098.25	415.945
495	S134	4406.25	415.945	529	DUMMY	4088.85	235.945
496	RX34	4396.85	235.945	530	S157	4079.55	325.945
497	S135	4387.55	325.945	531	S158	4070.25	415.945
498	S136	4378.25	415.945	532	RX40	4060.85	235.945
499	DUMMY	4368.85	235.945	533	S159	4051.55	325.945
500	S137	4359.55	325.945	534	S160	4042.25	415.945
501	S138	4350.25	415.945	535	DUMMY	4032.85	235.945
502	RX35	4340.85	235.945	536	S161	4023.55	325.945
503	S139	4331.55	325.945	537	S162	4014.25	415.945
504	S140	4322.25	415.945	538	RX41	4004.85	235.945
505	DUMMY	4312.85	235.945	539	S163	3995.55	325.945
506	S141	4303.55	325.945	540	S164	3986.25	415.945
507	S142	4294.25	415.945	541	DUMMY	3976.85	235.945
508	RX36	4284.85	235.945	542	S165	3967.55	325.945

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
543	S166	3958.25	415.945	577	DUMMY	3525.25	235.945
544	RX42	3948.85	235.945	578	S189	3515.95	325.945
545	S167	3939.55	325.945	579	S190	3506.65	415.945
546	S168	3930.25	415.945	580	RX48	3497.25	235.945
547	DUMMY	3920.85	235.945	581	S191	3487.95	325.945
548	S169	3911.55	325.945	582	S192	3478.65	415.945
549	S170	3902.25	415.945	583	DUMMY	3469.25	235.945
550	RX43	3892.85	235.945	584	S193	3459.95	325.945
551	S171	3883.55	325.945	585	S194	3450.65	415.945
552	S172	3874.25	415.945	586	RX49	3441.25	235.945
553	DUMMY	3864.85	235.945	587	S195	3431.95	325.945
554	S173	3855.55	325.945	588	S196	3422.65	415.945
555	S174	3846.25	415.945	589	DUMMY	3413.25	235.945
556	RX44	3836.85	235.945	590	S197	3403.95	325.945
557	S175	3827.55	325.945	591	S198	3394.65	415.945
558	S176	3818.25	415.945	592	RX50	3385.25	235.945
559	DUMMY	3808.85	235.945	593	S199	3375.95	325.945
560	S177	3799.55	325.945	594	S200	3366.65	415.945
561	S178	3790.25	415.945	595	DUMMY	3357.25	235.945
562	RX45	3780.85	235.945	596	S201	3347.95	325.945
563	S179	3771.55	325.945	597	S202	3338.65	415.945
564	S180	3762.25	415.945	598	RX51	3329.25	235.945
565	DUMMY	3637.25	235.945	599	S203	3319.95	325.945
566	S181	3627.95	325.945	600	S204	3310.65	415.945
567	S182	3618.65	415.945	601	DUMMY	3301.25	235.945
568	RX46	3609.25	235.945	602	S205	3291.95	325.945
569	S183	3599.95	325.945	603	S206	3282.65	415.945
570	S184	3590.65	415.945	604	RX52	3273.25	235.945
571	DUMMY	3581.25	235.945	605	S207	3263.95	325.945
572	S185	3571.95	325.945	606	S208	3254.65	415.945
573	S186	3562.65	415.945	607	DUMMY	3245.25	235.945
574	RX47	3553.25	235.945	608	S209	3235.95	325.945
575	S187	3543.95	325.945	609	S210	3226.65	415.945
576	S188	3534.65	415.945	610	RX53	3217.25	235.945

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
611	S211	3207.95	325.945	645	S234	2890.65	415.945
612	S212	3198.65	415.945	646	RX59	2881.25	235.945
613	DUMMY	3189.25	235.945	647	S235	2871.95	325.945
614	S213	3179.95	325.945	648	S236	2862.65	415.945
615	S214	3170.65	415.945	649	DUMMY	2853.25	235.945
616	RX54	3161.25	235.945	650	S237	2843.95	325.945
617	S215	3151.95	325.945	651	S238	2834.65	415.945
618	S216	3142.65	415.945	652	RX60	2825.25	235.945
619	DUMMY	3133.25	235.945	653	S239	2815.95	325.945
620	S217	3123.95	325.945	654	S240	2806.65	415.945
621	S218	3114.65	415.945	655	DUMMY	2797.25	235.945
622	RX55	3105.25	235.945	656	S241	2787.95	325.945
623	S219	3095.95	325.945	657	S242	2778.65	415.945
624	S220	3086.65	415.945	658	RX61	2769.25	235.945
625	DUMMY	3077.25	235.945	659	S243	2759.95	325.945
626	S221	3067.95	325.945	660	S244	2750.65	415.945
627	S222	3058.65	415.945	661	DUMMY	2741.25	235.945
628	RX56	3049.25	235.945	662	S245	2731.95	325.945
629	S223	3039.95	325.945	663	S246	2722.65	415.945
630	S224	3030.65	415.945	664	RX62	2713.25	235.945
631	DUMMY	3021.25	235.945	665	S247	2703.95	325.945
632	S225	3011.95	325.945	666	S248	2694.65	415.945
633	S226	3002.65	415.945	667	DUMMY	2685.25	235.945
634	RX57	2993.25	235.945	668	S249	2675.95	325.945
635	S227	2983.95	325.945	669	S250	2666.65	415.945
636	S228	2974.65	415.945	670	RX63	2657.25	235.945
637	DUMMY	2965.25	235.945	671	S251	2647.95	325.945
638	S229	2955.95	325.945	672	S252	2638.65	415.945
639	S230	2946.65	415.945	673	DUMMY	2629.25	235.945
640	RX58	2937.25	235.945	674	S253	2619.95	325.945
641	S231	2927.95	325.945	675	S254	2610.65	415.945
642	S232	2918.65	415.945	676	RX64	2601.25	235.945
643	DUMMY	2909.25	235.945	677	S255	2591.95	325.945
644	S233	2899.95	325.945	678	S256	2582.65	415.945

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
679	DUMMY	2573.25	235.945	713	S279	2255.95	325.945
680	S257	2563.95	325.945	714	S280	2246.65	415.945
681	S258	2554.65	415.945	715	DUMMY	2237.25	235.945
682	RX65	2545.25	235.945	716	S281	2227.95	325.945
683	S259	2535.95	325.945	717	S282	2218.65	415.945
684	S260	2526.65	415.945	718	RX71	2209.25	235.945
685	DUMMY	2517.25	235.945	719	S283	2199.95	325.945
686	S261	2507.95	325.945	720	S284	2190.65	415.945
687	S262	2498.65	415.945	721	DUMMY	2181.25	235.945
688	RX66	2489.25	235.945	722	S285	2171.95	325.945
689	S263	2479.95	325.945	723	S286	2162.65	415.945
690	S264	2470.65	415.945	724	RX72	2153.25	235.945
691	DUMMY	2461.25	235.945	725	S287	2143.95	325.945
692	S265	2451.95	325.945	726	S288	2134.65	415.945
693	S266	2442.65	415.945	727	DUMMY	2125.25	235.945
694	RX67	2433.25	235.945	728	S289	2115.95	325.945
695	S267	2423.95	325.945	729	S290	2106.65	415.945
696	S268	2414.65	415.945	730	RX73	2097.25	235.945
697	DUMMY	2405.25	235.945	731	S291	2087.95	325.945
698	S269	2395.95	325.945	732	S292	2078.65	415.945
699	S270	2386.65	415.945	733	DUMMY	2069.25	235.945
700	RX68	2377.25	235.945	734	S293	2059.95	325.945
701	S271	2367.95	325.945	735	S294	2050.65	415.945
702	S272	2358.65	415.945	736	RX74	2041.25	235.945
703	DUMMY	2349.25	235.945	737	S295	2031.95	325.945
704	S273	2339.95	325.945	738	S296	2022.65	415.945
705	S274	2330.65	415.945	739	DUMMY	2013.25	235.945
706	RX69	2321.25	235.945	740	S297	2003.95	325.945
707	S275	2311.95	325.945	741	S298	1994.65	415.945
708	S276	2302.65	415.945	742	RX75	1985.25	235.945
709	DUMMY	2293.25	235.945	743	S299	1975.95	325.945
710	S277	2283.95	325.945	744	S300	1966.65	415.945
711	S278	2274.65	415.945	745	DUMMY	1841.65	235.945
712	RX70	2265.25	235.945	746	S301	1832.35	325.945

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
747	S302	1823.05	415.945	781	DUMMY	1505.65	235.945
748	RX76	1813.65	235.945	782	S325	1496.35	325.945
749	S303	1804.35	325.945	783	S326	1487.05	415.945
750	S304	1795.05	415.945	784	RX82	1477.65	235.945
751	DUMMY	1785.65	235.945	785	S327	1468.35	325.945
752	S305	1776.35	325.945	786	S328	1459.05	415.945
753	S306	1767.05	415.945	787	DUMMY	1449.65	235.945
754	RX77	1757.65	235.945	788	S329	1440.35	325.945
755	S307	1748.35	325.945	789	S330	1431.05	415.945
756	S308	1739.05	415.945	790	RX83	1421.65	235.945
757	DUMMY	1729.65	235.945	791	S331	1412.35	325.945
758	S309	1720.35	325.945	792	S332	1403.05	415.945
759	S310	1711.05	415.945	793	DUMMY	1393.65	235.945
760	RX78	1701.65	235.945	794	S333	1384.35	325.945
761	S311	1692.35	325.945	795	S334	1375.05	415.945
762	S312	1683.05	415.945	796	RX84	1365.65	235.945
763	DUMMY	1673.65	235.945	797	S335	1356.35	325.945
764	S313	1664.35	325.945	798	S336	1347.05	415.945
765	S314	1655.05	415.945	799	DUMMY	1337.65	235.945
766	RX79	1645.65	235.945	800	S337	1328.35	325.945
767	S315	1636.35	325.945	801	S338	1319.05	415.945
768	S316	1627.05	415.945	802	RX85	1309.65	235.945
769	DUMMY	1617.65	235.945	803	S339	1300.35	325.945
770	S317	1608.35	325.945	804	S340	1291.05	415.945
771	S318	1599.05	415.945	805	DUMMY	1281.65	235.945
772	RX80	1589.65	235.945	806	S341	1272.35	325.945
773	S319	1580.35	325.945	807	S342	1263.05	415.945
774	S320	1571.05	415.945	808	RX86	1253.65	235.945
775	DUMMY	1561.65	235.945	809	S343	1244.35	325.945
776	S321	1552.35	325.945	810	S344	1235.05	415.945
777	S322	1543.05	415.945	811	DUMMY	1225.65	235.945
778	RX81	1533.65	235.945	812	S345	1216.35	325.945
779	S323	1524.35	325.945	813	S346	1207.05	415.945
780	S324	1515.05	415.945	814	RX87	1197.65	235.945

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
815	S347	1188.35	325.945	849	S370	871.05	415.945
816	S348	1179.05	415.945	850	RX93	861.65	235.945
817	DUMMY	1169.65	235.945	851	S371	852.35	325.945
818	S349	1160.35	325.945	852	S372	843.05	415.945
819	S350	1151.05	415.945	853	DUMMY	833.65	235.945
820	RX88	1141.65	235.945	854	S373	824.35	325.945
821	S351	1132.35	325.945	855	S374	815.05	415.945
822	S352	1123.05	415.945	856	RX94	805.65	235.945
823	DUMMY	1113.65	235.945	857	S375	796.35	325.945
824	S353	1104.35	325.945	858	S376	787.05	415.945
825	S354	1095.05	415.945	859	DUMMY	777.65	235.945
826	RX89	1085.65	235.945	860	S377	768.35	325.945
827	S355	1076.35	325.945	861	S378	759.05	415.945
828	S356	1067.05	415.945	862	RX95	749.65	235.945
829	DUMMY	1057.65	235.945	863	S379	740.35	325.945
830	S357	1048.35	325.945	864	S380	731.05	415.945
831	S358	1039.05	415.945	865	DUMMY	721.65	235.945
832	RX90	1029.65	235.945	866	S381	712.35	325.945
833	S359	1020.35	325.945	867	S382	703.05	415.945
834	S360	1011.05	415.945	868	RX96	693.65	235.945
835	DUMMY	1001.65	235.945	869	S383	684.35	325.945
836	S361	992.35	325.945	870	S384	675.05	415.945
837	S362	983.05	415.945	871	DUMMY	665.65	235.945
838	RX91	973.65	235.945	872	S385	656.35	325.945
839	S363	964.35	325.945	873	S386	647.05	415.945
840	S364	955.05	415.945	874	RX97	637.65	235.945
841	DUMMY	945.65	235.945	875	S387	628.35	325.945
842	S365	936.35	325.945	876	S388	619.05	415.945
843	S366	927.05	415.945	877	DUMMY	609.65	235.945
844	RX92	917.65	235.945	878	S389	600.35	325.945
845	S367	908.35	325.945	879	S390	591.05	415.945
846	S368	899.05	415.945	880	RX98	581.65	235.945
847	DUMMY	889.65	235.945	881	S391	572.35	325.945
848	S369	880.35	325.945	882	S392	563.05	415.945

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
883	DUMMY	553.65	235.945	917	S415	236.35	325.945
884	S393	544.35	325.945	918	S416	227.05	415.945
885	S394	535.05	415.945	919	DUMMY	217.65	235.945
886	RX99	525.65	235.945	920	S417	208.35	325.945
887	S395	516.35	325.945	921	S418	199.05	415.945
888	S396	507.05	415.945	922	RX105	189.65	235.945
889	DUMMY	497.65	235.945	923	S419	180.35	325.945
890	S397	488.35	325.945	924	S420	171.05	415.945
891	S398	479.05	415.945	925	DUMMY	-171.05	235.945
892	RX100	469.65	235.945	926	S421	-180.35	325.945
893	S399	460.35	325.945	927	S422	-189.65	415.945
894	S400	451.05	415.945	928	RX106	-199.05	235.945
895	DUMMY	441.65	235.945	929	S423	-208.35	325.945
896	S401	432.35	325.945	930	S424	-217.65	415.945
897	S402	423.05	415.945	931	DUMMY	-227.05	235.945
898	RX101	413.65	235.945	932	S425	-236.35	325.945
899	S403	404.35	325.945	933	S426	-245.65	415.945
900	S404	395.05	415.945	934	RX107	-255.05	235.945
901	DUMMY	385.65	235.945	935	S427	-264.35	325.945
902	S405	376.35	325.945	936	S428	-273.65	415.945
903	S406	367.05	415.945	937	DUMMY	-283.05	235.945
904	RX102	357.65	235.945	938	S429	-292.35	325.945
905	S407	348.35	325.945	939	S430	-301.65	415.945
906	S408	339.05	415.945	940	RX108	-311.05	235.945
907	DUMMY	329.65	235.945	941	S431	-320.35	325.945
908	S409	320.35	325.945	942	S432	-329.65	415.945
909	S410	311.05	415.945	943	DUMMY	-339.05	235.945
910	RX103	301.65	235.945	944	S433	-348.35	325.945
911	S411	292.35	325.945	945	S434	-357.65	415.945
912	S412	283.05	415.945	946	RX109	-367.05	235.945
913	DUMMY	273.65	235.945	947	S435	-376.35	325.945
914	S413	264.35	325.945	948	S436	-385.65	415.945
915	S414	255.05	415.945	949	DUMMY	-395.05	235.945
916	RX104	245.65	235.945	950	S437	-404.35	325.945

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
951	S438	-413.65	415.945	985	DUMMY	-731.05	235.945
952	RX110	-423.05	235.945	986	S461	-740.35	325.945
953	S439	-432.35	325.945	987	S462	-749.65	415.945
954	S440	-441.65	415.945	988	RX116	-759.05	235.945
955	DUMMY	-451.05	235.945	989	S463	-768.35	325.945
956	S441	-460.35	325.945	990	S464	-777.65	415.945
957	S442	-469.65	415.945	991	DUMMY	-787.05	235.945
958	RX111	-479.05	235.945	992	S465	-796.35	325.945
959	S443	-488.35	325.945	993	S466	-805.65	415.945
960	S444	-497.65	415.945	994	RX117	-815.05	235.945
961	DUMMY	-507.05	235.945	995	S467	-824.35	325.945
962	S445	-516.35	325.945	996	S468	-833.65	415.945
963	S446	-525.65	415.945	997	DUMMY	-843.05	235.945
964	RX112	-535.05	235.945	998	S469	-852.35	325.945
965	S447	-544.35	325.945	999	S470	-861.65	415.945
966	S448	-553.65	415.945	1000	RX118	-871.05	235.945
967	DUMMY	-563.05	235.945	1001	S471	-880.35	325.945
968	S449	-572.35	325.945	1002	S472	-889.65	415.945
969	S450	-581.65	415.945	1003	DUMMY	-899.05	235.945
970	RX113	-591.05	235.945	1004	S473	-908.35	325.945
971	S451	-600.35	325.945	1005	S474	-917.65	415.945
972	S452	-609.65	415.945	1006	RX119	-927.05	235.945
973	DUMMY	-619.05	235.945	1007	S475	-936.35	325.945
974	S453	-628.35	325.945	1008	S476	-945.65	415.945
975	S454	-637.65	415.945	1009	DUMMY	-955.05	235.945
976	RX114	-647.05	235.945	1010	S477	-964.35	325.945
977	S455	-656.35	325.945	1011	S478	-973.65	415.945
978	S456	-665.65	415.945	1012	RX120	-983.05	235.945
979	DUMMY	-675.05	235.945	1013	S479	-992.35	325.945
980	S457	-684.35	325.945	1014	S480	-1001.65	415.945
981	S458	-693.65	415.945	1015	DUMMY	-1011.05	235.945
982	RX115	-703.05	235.945	1016	S481	-1020.35	325.945
983	S459	-712.35	325.945	1017	S482	-1029.65	415.945
984	S460	-721.65	415.945	1018	RX121	-1039.05	235.945

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1019	S483	-1048.35	325.945	1053	RX127	-1375.05	235.945
1020	S484	-1057.65	415.945	1054	S507	-1384.35	325.945
1021	DUMMY	-1067.05	235.945	1055	S508	-1393.65	415.945
1022	S485	-1076.35	325.945	1056	DUMMY	-1403.05	235.945
1023	S486	-1085.65	415.945	1057	S509	-1412.35	325.945
1024	RX122	-1095.05	235.945	1058	S510	-1421.65	415.945
1025	S487	-1104.35	325.945	1059	RX128	-1431.05	235.945
1026	S488	-1113.65	415.945	1060	S511	-1440.35	325.945
1027	DUMMY	-1123.05	235.945	1061	S512	-1449.65	415.945
1028	S489	-1132.35	325.945	1062	DUMMY	-1459.05	235.945
1029	S490	-1141.65	415.945	1063	S513	-1468.35	325.945
1030	RX123	-1151.05	235.945	1064	S514	-1477.65	415.945
1031	S491	-1160.35	325.945	1065	RX129	-1487.05	235.945
1032	S492	-1169.65	415.945	1066	S515	-1496.35	325.945
1033	DUMMY	-1179.05	235.945	1067	S516	-1505.65	415.945
1034	S493	-1188.35	325.945	1068	DUMMY	-1515.05	235.945
1035	S494	-1197.65	415.945	1069	S517	-1524.35	325.945
1036	RX124	-1207.05	235.945	1070	S518	-1533.65	415.945
1037	S495	-1216.35	325.945	1071	RX130	-1543.05	235.945
1038	S496	-1225.65	415.945	1072	S519	-1552.35	325.945
1039	DUMMY	-1235.05	235.945	1073	S520	-1561.65	415.945
1040	S497	-1244.35	325.945	1074	DUMMY	-1571.05	235.945
1041	S498	-1253.65	415.945	1075	S521	-1580.35	325.945
1042	RX125	-1263.05	235.945	1076	S522	-1589.65	415.945
1043	S499	-1272.35	325.945	1077	RX131	-1599.05	235.945
1044	S500	-1281.65	415.945	1078	S523	-1608.35	325.945
1045	DUMMY	-1291.05	235.945	1079	S524	-1617.65	415.945
1046	S501	-1300.35	325.945	1080	DUMMY	-1627.05	235.945
1047	S502	-1309.65	415.945	1081	S525	-1636.35	325.945
1048	RX126	-1319.05	235.945	1082	S526	-1645.65	415.945
1049	S503	-1328.35	325.945	1083	RX132	-1655.05	235.945
1050	S504	-1337.65	415.945	1084	S527	-1664.35	325.945
1051	DUMMY	-1347.05	235.945	1085	S528	-1673.65	415.945
1052	S505	-1356.35	325.945	1086	RX127	-1375.05	235.945

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1087	DUMMY	-1683.05	235.945	1121	S551	-2115.95	325.945
1088	S529	-1692.35	325.945	1122	S552	-2125.25	415.945
1089	S530	-1701.65	415.945	1123	DUMMY	-2134.65	235.945
1090	RX133	-1711.05	235.945	1124	S553	-2143.95	325.945
1091	S531	-1720.35	325.945	1125	S554	-2153.25	415.945
1092	S532	-1729.65	415.945	1126	RX139	-2162.65	235.945
1093	DUMMY	-1739.05	235.945	1127	S555	-2171.95	325.945
1094	S533	-1748.35	325.945	1128	S556	-2181.25	415.945
1095	S534	-1757.65	415.945	1129	DUMMY	-2190.65	235.945
1096	RX134	-1767.05	235.945	1130	S557	-2199.95	325.945
1097	S535	-1776.35	325.945	1131	S558	-2209.25	415.945
1098	S536	-1785.65	415.945	1132	RX140	-2218.65	235.945
1099	DUMMY	-1795.05	235.945	1133	S559	-2227.95	325.945
1100	S537	-1804.35	325.945	1134	S560	-2237.25	415.945
1101	S538	-1813.65	415.945	1135	DUMMY	-2246.65	235.945
1102	RX135	-1823.05	235.945	1136	S561	-2255.95	325.945
1103	S539	-1832.35	325.945	1137	S562	-2265.25	415.945
1104	S540	-1841.65	415.945	1138	RX141	-2274.65	235.945
1105	DUMMY	-1966.65	235.945	1139	S563	-2283.95	325.945
1106	S541	-1975.95	325.945	1140	S564	-2293.25	415.945
1107	S542	-1985.25	415.945	1141	DUMMY	-2302.65	235.945
1108	RX136	-1994.65	235.945	1142	S565	-2311.95	325.945
1109	S543	-2003.95	325.945	1143	S566	-2321.25	415.945
1110	S544	-2013.25	415.945	1144	RX142	-2330.65	235.945
1111	DUMMY	-2022.65	235.945	1145	S567	-2339.95	325.945
1112	S545	-2031.95	325.945	1146	S568	-2349.25	415.945
1113	S546	-2041.25	415.945	1147	DUMMY	-2358.65	235.945
1114	RX137	-2050.65	235.945	1148	S569	-2367.95	325.945
1115	S547	-2059.95	325.945	1149	S570	-2377.25	415.945
1116	S548	-2069.25	415.945	1150	RX143	-2386.65	235.945
1117	DUMMY	-2078.65	235.945	1151	S571	-2395.95	325.945
1118	S549	-2087.95	325.945	1152	S572	-2405.25	415.945
1119	S550	-2097.25	415.945	1153	DUMMY	-2414.65	235.945
1120	RX138	-2106.65	235.945	1154	S573	-2423.95	325.945

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1155	S574	-2433.25	415.945	1189	DUMMY	-2750.65	235.945
1156	RX144	-2442.65	235.945	1190	S597	-2759.95	325.945
1157	S575	-2451.95	325.945	1191	S598	-2769.25	415.945
1158	S576	-2461.25	415.945	1192	RX150	-2778.65	235.945
1159	DUMMY	-2470.65	235.945	1193	S599	-2787.95	325.945
1160	S577	-2479.95	325.945	1194	S600	-2797.25	415.945
1161	S578	-2489.25	415.945	1195	DUMMY	-2806.65	235.945
1162	RX145	-2498.65	235.945	1196	S601	-2815.95	325.945
1163	S579	-2507.95	325.945	1197	S602	-2825.25	415.945
1164	S580	-2517.25	415.945	1198	RX151	-2834.65	235.945
1165	DUMMY	-2526.65	235.945	1199	S603	-2843.95	325.945
1166	S581	-2535.95	325.945	1200	S604	-2853.25	415.945
1167	S582	-2545.25	415.945	1201	DUMMY	-2862.65	235.945
1168	RX146	-2554.65	235.945	1202	S605	-2871.95	325.945
1169	S583	-2563.95	325.945	1203	S606	-2881.25	415.945
1170	S584	-2573.25	415.945	1204	RX152	-2890.65	235.945
1171	DUMMY	-2582.65	235.945	1205	S607	-2899.95	325.945
1172	S585	-2591.95	325.945	1206	S608	-2909.25	415.945
1173	S586	-2601.25	415.945	1207	DUMMY	-2918.65	235.945
1174	RX147	-2610.65	235.945	1208	S609	-2927.95	325.945
1175	S587	-2619.95	325.945	1209	S610	-2937.25	415.945
1176	S588	-2629.25	415.945	1210	RX153	-2946.65	235.945
1177	DUMMY	-2638.65	235.945	1211	S611	-2955.95	325.945
1178	S589	-2647.95	325.945	1212	S612	-2965.25	415.945
1179	S590	-2657.25	415.945	1213	DUMMY	-2974.65	235.945
1180	RX148	-2666.65	235.945	1214	S613	-2983.95	325.945
1181	S591	-2675.95	325.945	1215	S614	-2993.25	415.945
1182	S592	-2685.25	415.945	1216	RX154	-3002.65	235.945
1183	DUMMY	-2694.65	235.945	1217	S615	-3011.95	325.945
1184	S593	-2703.95	325.945	1218	S616	-3021.25	415.945
1185	S594	-2713.25	415.945	1219	DUMMY	-3030.65	235.945
1186	RX149	-2722.65	235.945	1220	S617	-3039.95	325.945
1187	S595	-2731.95	325.945	1221	S618	-3049.25	415.945
1188	S596	-2741.25	415.945	1222	RX155	-3058.65	235.945

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1223	S619	-3067.95	325.945	1257	S642	-3385.25	415.945
1224	S620	-3077.25	415.945	1258	RX161	-3394.65	235.945
1225	DUMMY	-3086.65	235.945	1259	S643	-3403.95	325.945
1226	S621	-3095.95	325.945	1260	S644	-3413.25	415.945
1227	S622	-3105.25	415.945	1261	DUMMY	-3422.65	235.945
1228	RX156	-3114.65	235.945	1262	S645	-3431.95	325.945
1229	S623	-3123.95	325.945	1263	S646	-3441.25	415.945
1230	S624	-3133.25	415.945	1264	RX162	-3450.65	235.945
1231	DUMMY	-3142.65	235.945	1265	S647	-3459.95	325.945
1232	S625	-3151.95	325.945	1266	S648	-3469.25	415.945
1233	S626	-3161.25	415.945	1267	DUMMY	-3478.65	235.945
1234	RX157	-3170.65	235.945	1268	S649	-3487.95	325.945
1235	S627	-3179.95	325.945	1269	S650	-3497.25	415.945
1236	S628	-3189.25	415.945	1270	RX163	-3506.65	235.945
1237	DUMMY	-3198.65	235.945	1271	S651	-3515.95	325.945
1238	S629	-3207.95	325.945	1272	S652	-3525.25	415.945
1239	S630	-3217.25	415.945	1273	DUMMY	-3534.65	235.945
1240	RX158	-3226.65	235.945	1274	S653	-3543.95	325.945
1241	S631	-3235.95	325.945	1275	S654	-3553.25	415.945
1242	S632	-3245.25	415.945	1276	RX164	-3562.65	235.945
1243	DUMMY	-3254.65	235.945	1277	S655	-3571.95	325.945
1244	S633	-3263.95	325.945	1278	S656	-3581.25	415.945
1245	S634	-3273.25	415.945	1279	DUMMY	-3590.65	235.945
1246	RX159	-3282.65	235.945	1280	S657	-3599.95	325.945
1247	S635	-3291.95	325.945	1281	S658	-3609.25	415.945
1248	S636	-3301.25	415.945	1282	RX165	-3618.65	235.945
1249	DUMMY	-3310.65	235.945	1283	S659	-3627.95	325.945
1250	S637	-3319.95	325.945	1284	S660	-3637.25	415.945
1251	S638	-3329.25	415.945	1285	DUMMY	-3762.25	235.945
1252	RX160	-3338.65	235.945	1286	S661	-3771.55	325.945
1253	S639	-3347.95	325.945	1287	S662	-3780.85	415.945
1254	S640	-3357.25	415.945	1288	RX166	-3790.25	235.945
1255	DUMMY	-3366.65	235.945	1289	S663	-3799.55	325.945
1256	S641	-3375.95	325.945	1290	S664	-3808.85	415.945

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1291	DUMMY	-3818.25	235.945	1325	S687	-4135.55	325.945
1292	S665	-3827.55	325.945	1326	S688	-4144.85	415.945
1293	S666	-3836.85	415.945	1327	DUMMY	-4154.25	235.945
1294	RX167	-3846.25	235.945	1328	S689	-4163.55	325.945
1295	S667	-3855.55	325.945	1329	S690	-4172.85	415.945
1296	S668	-3864.85	415.945	1330	RX173	-4182.25	235.945
1297	DUMMY	-3874.25	235.945	1331	S691	-4191.55	325.945
1298	S669	-3883.55	325.945	1332	S692	-4200.85	415.945
1299	S670	-3892.85	415.945	1333	DUMMY	-4210.25	235.945
1300	RX168	-3902.25	235.945	1334	S693	-4219.55	325.945
1301	S671	-3911.55	325.945	1335	S694	-4228.85	415.945
1302	S672	-3920.85	415.945	1336	RX174	-4238.25	235.945
1303	DUMMY	-3930.25	235.945	1337	S695	-4247.55	325.945
1304	S673	-3939.55	325.945	1338	S696	-4256.85	415.945
1305	S674	-3948.85	415.945	1339	DUMMY	-4266.25	235.945
1306	RX169	-3958.25	235.945	1340	S697	-4275.55	325.945
1307	S675	-3967.55	325.945	1341	S698	-4284.85	415.945
1308	S676	-3976.85	415.945	1342	RX175	-4294.25	235.945
1309	DUMMY	-3986.25	235.945	1343	S699	-4303.55	325.945
1310	S677	-3995.55	325.945	1344	S700	-4312.85	415.945
1311	S678	-4004.85	415.945	1345	DUMMY	-4322.25	235.945
1312	RX170	-4014.25	235.945	1346	S701	-4331.55	325.945
1313	S679	-4023.55	325.945	1347	S702	-4340.85	415.945
1314	S680	-4032.85	415.945	1348	RX176	-4350.25	235.945
1315	DUMMY	-4042.25	235.945	1349	S703	-4359.55	325.945
1316	S681	-4051.55	325.945	1350	S704	-4368.85	415.945
1317	S682	-4060.85	415.945	1351	DUMMY	-4378.25	235.945
1318	RX171	-4070.25	235.945	1352	S705	-4387.55	325.945
1319	S683	-4079.55	325.945	1353	S706	-4396.85	415.945
1320	S684	-4088.85	415.945	1354	RX177	-4406.25	235.945
1321	DUMMY	-4098.25	235.945	1355	S707	-4415.55	325.945
1322	S685	-4107.55	325.945	1356	S708	-4424.85	415.945
1323	S686	-4116.85	415.945	1357	DUMMY	-4434.25	235.945
1324	RX172	-4126.25	235.945	1358	S709	-4443.55	325.945

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1359	S710	-4452.85	415.945	1393	DUMMY	-4770.25	235.945
1360	RX178	-4462.25	235.945	1394	S733	-4779.55	325.945
1361	S711	-4471.55	325.945	1395	S734	-4788.85	415.945
1362	S712	-4480.85	415.945	1396	RX184	-4798.25	235.945
1363	DUMMY	-4490.25	235.945	1397	S735	-4807.55	325.945
1364	S713	-4499.55	325.945	1398	S736	-4816.85	415.945
1365	S714	-4508.85	415.945	1399	DUMMY	-4826.25	235.945
1366	RX179	-4518.25	235.945	1400	S737	-4835.55	325.945
1367	S715	-4527.55	325.945	1401	S738	-4844.85	415.945
1368	S716	-4536.85	415.945	1402	RX185	-4854.25	235.945
1369	DUMMY	-4546.25	235.945	1403	S739	-4863.55	325.945
1370	S717	-4555.55	325.945	1404	S740	-4872.85	415.945
1371	S718	-4564.85	415.945	1405	DUMMY	-4882.25	235.945
1372	RX180	-4574.25	235.945	1406	S741	-4891.55	325.945
1373	S719	-4583.55	325.945	1407	S742	-4900.85	415.945
1374	S720	-4592.85	415.945	1408	RX186	-4910.25	235.945
1375	DUMMY	-4602.25	235.945	1409	S743	-4919.55	325.945
1376	S721	-4611.55	325.945	1410	S744	-4928.85	415.945
1377	S722	-4620.85	415.945	1411	DUMMY	-4938.25	235.945
1378	RX181	-4630.25	235.945	1412	S745	-4947.55	325.945
1379	S723	-4639.55	325.945	1413	S746	-4956.85	415.945
1380	S724	-4648.85	415.945	1414	RX187	-4966.25	235.945
1381	DUMMY	-4658.25	235.945	1415	S747	-4975.55	325.945
1382	S725	-4667.55	325.945	1416	S748	-4984.85	415.945
1383	S726	-4676.85	415.945	1417	DUMMY	-4994.25	235.945
1384	RX182	-4686.25	235.945	1418	S749	-5003.55	325.945
1385	S727	-4695.55	325.945	1419	S750	-5012.85	415.945
1386	S728	-4704.85	415.945	1420	RX188	-5022.25	235.945
1387	DUMMY	-4714.25	235.945	1421	S751	-5031.55	325.945
1388	S729	-4723.55	325.945	1422	S752	-5040.85	415.945
1389	S730	-4732.85	415.945	1423	DUMMY	-5050.25	235.945
1390	RX183	-4742.25	235.945	1424	S753	-5059.55	325.945
1391	S731	-4751.55	325.945	1425	S754	-5068.85	415.945
1392	S732	-4760.85	415.945	1426	RX189	-5078.25	235.945

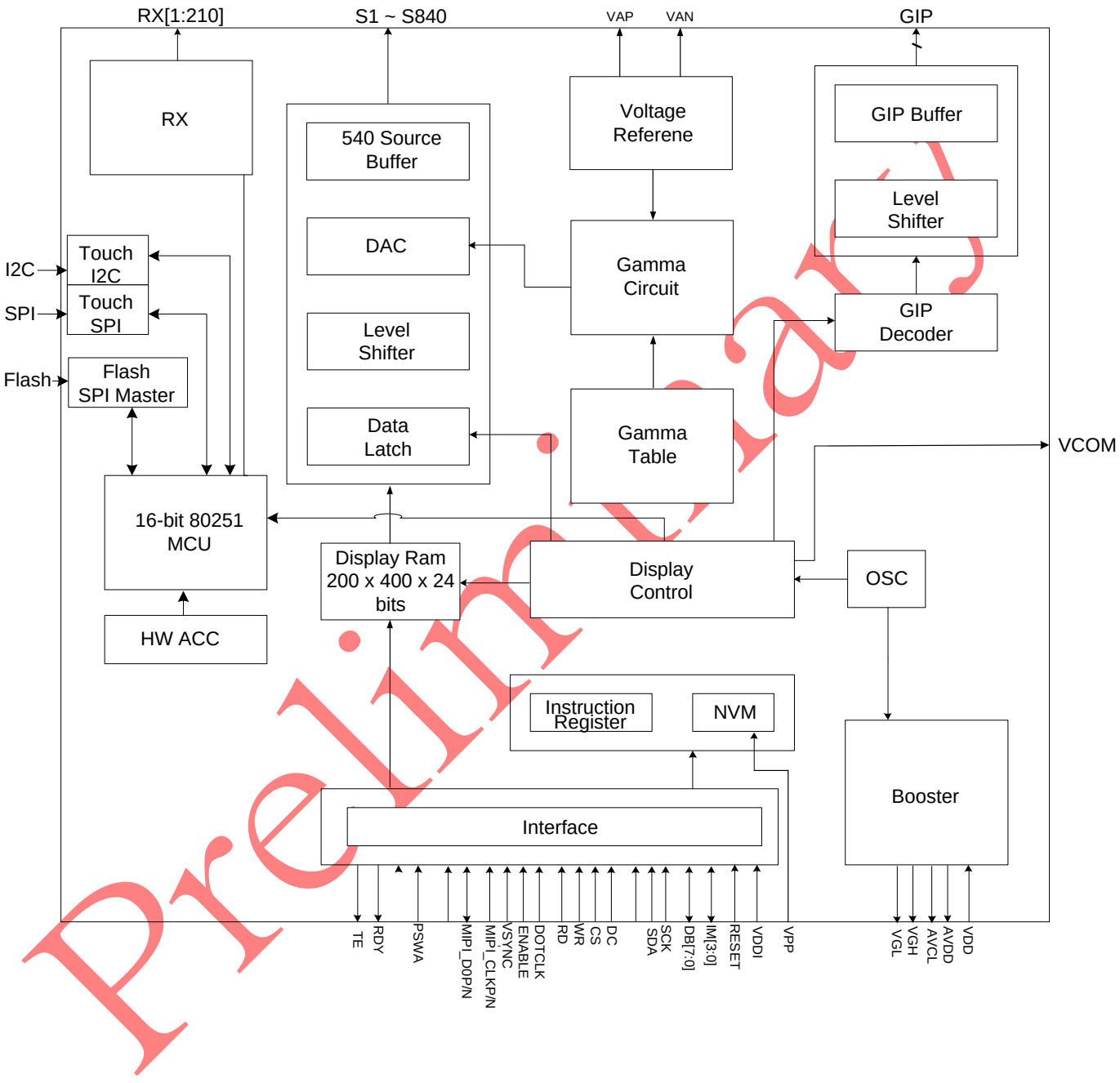
PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1427	S755	-5087.55	325.945	1461	S778	-5404.85	415.945
1428	S756	-5096.85	415.945	1462	RX195	-5414.25	235.945
1429	DUMMY	-5106.25	235.945	1463	S779	-5423.55	325.945
1430	S757	-5115.55	325.945	1464	S780	-5432.85	415.945
1431	S758	-5124.85	415.945	1465	DUMMY	-5557.85	235.945
1432	RX190	-5134.25	235.945	1466	S781	-5567.15	325.945
1433	S759	-5143.55	325.945	1467	S782	-5576.45	415.945
1434	S760	-5152.85	415.945	1468	RX196	-5585.85	235.945
1435	DUMMY	-5162.25	235.945	1469	S783	-5595.15	325.945
1436	S761	-5171.55	325.945	1470	S784	-5604.45	415.945
1437	S762	-5180.85	415.945	1471	DUMMY	-5613.85	235.945
1438	RX191	-5190.25	235.945	1472	S785	-5623.15	325.945
1439	S763	-5199.55	325.945	1473	S786	-5632.45	415.945
1440	S764	-5208.85	415.945	1474	RX197	-5641.85	235.945
1441	DUMMY	-5218.25	235.945	1475	S787	-5651.15	325.945
1442	S765	-5227.55	325.945	1476	S788	-5660.45	415.945
1443	S766	-5236.85	415.945	1477	DUMMY	-5669.85	235.945
1444	RX192	-5246.25	235.945	1478	S789	-5679.15	325.945
1445	S767	-5255.55	325.945	1479	S790	-5688.45	415.945
1446	S768	-5264.85	415.945	1480	RX198	-5697.85	235.945
1447	DUMMY	-5274.25	235.945	1481	S791	-5707.15	325.945
1448	S769	-5283.55	325.945	1482	S792	-5716.45	415.945
1449	S770	-5292.85	415.945	1483	DUMMY	-5725.85	235.945
1450	RX193	-5302.25	235.945	1484	S793	-5735.15	325.945
1451	S771	-5311.55	325.945	1485	S794	-5744.45	415.945
1452	S772	-5320.85	415.945	1486	RX199	-5753.85	235.945
1453	DUMMY	-5330.25	235.945	1487	S795	-5763.15	325.945
1454	S773	-5339.55	325.945	1488	S796	-5772.45	415.945
1455	S774	-5348.85	415.945	1489	DUMMY	-5781.85	235.945
1456	RX194	-5358.25	235.945	1490	S797	-5791.15	325.945
1457	S775	-5367.55	325.945	1491	S798	-5800.45	415.945
1458	S776	-5376.85	415.945	1492	RX200	-5809.85	235.945
1459	DUMMY	-5386.25	235.945	1493	S799	-5819.15	325.945
1460	S777	-5395.55	325.945	1494	S800	-5828.45	415.945

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1495	DUMMY	-5837.85	235.945	1529	S823	-6155.15	325.945
1496	S801	-5847.15	325.945	1530	S824	-6164.45	415.945
1497	S802	-5856.45	415.945	1531	DUMMY	-6173.85	235.945
1498	RX201	-5865.85	235.945	1532	S825	-6183.15	325.945
1499	S803	-5875.15	325.945	1533	S826	-6192.45	415.945
1500	S804	-5884.45	415.945	1534	RX207	-6201.85	235.945
1501	DUMMY	-5893.85	235.945	1535	S827	-6211.15	325.945
1502	S805	-5903.15	325.945	1536	S828	-6220.45	415.945
1503	S806	-5912.45	415.945	1537	DUMMY	-6229.85	235.945
1504	RX202	-5921.85	235.945	1538	S829	-6239.15	325.945
1505	S807	-5931.15	325.945	1539	S830	-6248.45	415.945
1506	S808	-5940.45	415.945	1540	RX208	-6257.85	235.945
1507	DUMMY	-5949.85	235.945	1541	S831	-6267.15	325.945
1508	S809	-5959.15	325.945	1542	S832	-6276.45	415.945
1509	S810	-5968.45	415.945	1543	DUMMY	-6285.85	235.945
1510	RX203	-5977.85	235.945	1544	S833	-6295.15	325.945
1511	S811	-5987.15	325.945	1545	S834	-6304.45	415.945
1512	S812	-5996.45	415.945	1546	RX209	-6313.85	235.945
1513	DUMMY	-6005.85	235.945	1547	S835	-6323.15	325.945
1514	S813	-6015.15	325.945	1548	S836	-6332.45	415.945
1515	S814	-6024.45	415.945	1549	DUMMY	-6341.85	235.945
1516	RX204	-6033.85	235.945	1550	S837	-6351.15	325.945
1517	S815	-6043.15	325.945	1551	S838	-6360.45	415.945
1518	S816	-6052.45	415.945	1552	RX210	-6369.85	235.945
1519	DUMMY	-6061.85	235.945	1553	S839	-6379.15	325.945
1520	S817	-6071.15	325.945	1554	S840	-6388.45	415.945
1521	S818	-6080.45	415.945	1555	GOL[12]	-6530.35	325.945
1522	RX205	-6089.85	235.945	1556	GOL[11]	-6544.35	415.945
1523	S819	-6099.15	325.945	1557	GOL[10]	-6558.35	325.945
1524	S820	-6108.45	415.945	1558	GOL[9]	-6572.35	415.945
1525	DUMMY	-6117.85	235.945	1559	GOL[8]	-6586.35	325.945
1526	S821	-6127.15	325.945	1560	GOL[7]	-6600.35	415.945
1527	S822	-6136.45	415.945	1561	GOL[6]	-6614.35	325.945
1528	RX206	-6145.85	235.945	1562	GOL[5]	-6628.35	415.945

PAD No.	PIN Name	X	Y
1563	GOL[4]	-6642.35	325.945
1564	GOL[3]	-6656.35	415.945
1565	GOL[2]	-6670.35	325.945
1566	GOL[1]	-6684.35	415.945
1567	VGHO	-6698.350	325.945
1568	VGLO	-6712.350	415.945

Note: The Pad Location is not include the Temperature Compensation (TC)

5 BLOCK DIAGRAM



6 PIN DESCRIPTION

6.1 Power Supply Pins

Name	I/O	Description	Connect Pin
VDD	I	- Power Supply for Analog, Digital System and Booster Circuit.	VDD
VDD_VH	I	- Power Supply for internal Circuit.	VDD
VDDI	I	- Power Supply for I/O System. - VDDI must be lower than or equal to VDD.	VDDI
GND, GND1, GND_VEE	I	- System Ground for Analog System, Digital System, I/O System and Booster Circuit.	GND
VPP	I	- Power Supply for Internal NVM. - When programming NVM, It needs external power supply voltage (7.5V). - The current of Ivpp must be more than 10mA. - If select internal power then leaves these pins open when not on use.	External Power

6.2 Interface Logic Pins

Name	I/O	Description	Connect Pin
IM2P IM1P IM0P	I	-The System interface mode select.	GND/VDDI
RESX	I	-Global reset signal	MCU
TE	O	-Tearing effect output pin to synchronies MCU to frame writing, activated by S/W command. When this pin is not activated (TE function OFF), this pin is GND level. -If not used, please let this pin open.	MCU
D[7:0]	I/O	-D[7:0] are used as MCU parallel interface data bus, RGB interface data bus.	MCU

IM2	IM1	IM0	MPU Interface Mode	Data pin
0	0	0	3-line 9bit serial I/F	SDA: in/out
0	0	1	4-line 8bit serial I/F	SDA: in/out
0	1	0	2 data lane serial I/F	SDA0: in/out、SDA1: in
0	1	1	QSPI I/F	SDA[3:0]: in/out
1	0	0	RGB_3-line 9bit serial I/F	SDA: in/out、DB[7:0]
1	0	1	RGB_4-line 8bit serial I/F	SDA: in/out、DB[7:0]
1	1	0	MIPI I/F	DP/DN
1	1	1	80-8bit parallel I/F	DB[7:0]

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Connect Pin</th></tr>
<tr><td></td><td></td><td>-D[1:0] are used as QSPI interface data bus. (SDA2、SDA3)
-If not used, please fix this pin at GND.</td><td></td></tr>
<tr><td>SDA</td><td>I/O</td><td>-Data pin
- SDA signal in 3-line serial ,4-line serial , RGB 3-line ,RGB 4-line
- SDA0 signal in 2 data lane serial ,QSPI (SDA0)
-If not used, please fix this pin at GND.</td><td>MCU</td></tr>
<tr><td>CSX</td><td>I</td><td>-Chip select pin.
CSX=’0’ : Low enable.
CSX=’1’ : High disable
-If not used, please fix this pin at VDDI.</td><td>MCU</td></tr>
<tr><td>DCX</td><td>I</td><td>-Display data/command selection pin in parallel interface.
DCX=’1’: display data or parameter.
DCX=’0’: command data.
-Display data/command selection pin in 4-line serial interface. (A0)
DCX=’1’: display data or parameter.
DCX=’0’: command data.
-SDA1 signal in 2 data lane serial interface. (SDA1)
-If not used, please fix this pin at VDDI.</td><td>MCU</td></tr>
<tr><td>WRX</td><td>I</td><td>-Write enable in MCU parallel interface.
- Dot clock signal in RGB interface. (DOTCLK)
-If not used, please fix this pin at VDDI</td><td>MCU</td></tr>
<tr><td>RDX</td><td>I</td><td>-Read enable in MCU parallel interface.
-SCL signal in 3-line serial ,4-line serial , RGB 3-line ,RGB 4-line, 2 data lane serial ,QSPI (SCL)
-If not used, please fix this pin at VDDI.</td><td>MCU</td></tr>
<tr><td>DE</td><td>I</td><td>-Data enable signal in RGB interface
-If not used, please fix this pin at VDDI.</td><td>MCU</td></tr>
<tr><td>HSYNC</td><td>I</td><td>-Horizontal (Line) synchronizing input signal in RGB interface.
-If not used, please fix to the VDDI.</td><td>MCU</td></tr>
<tr><td>VSYNC</td><td>I</td><td>-Vertical (Frame) synchronizing input signal in RGB interface.
-If not used, please fix to the VDDI.</td><td>MCU</td></tr>
<tr><td>PSWA</td><td>I</td><td>-Differential clock polarity swap in MIPI-DSI interface.
-If not used, please fix to the GND.
<table>
<tr><th rowspan="2">PSWA</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th colspan="4">MIPI I/F</th></tr>
<tr><th>HSCP</th><th>HSCN</th><th>HSD0P</th><th>HSD0N</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>HSCP</td><td>HSCN</td><td>HSD0P</td><td>HSD0N</td></tr>
</table></td><td>GND/VDDI</td></tr>
</table>

Name	I/O	Description	Connect Pin
		1 | | | | HSCN | HSCP | HSD0N | HSD0P	
HSCP	I	-MIPI-DSI clock lane positive-end input pin. -If not used, please fix this pin at GND.	MCU
HSCN	I	-MIPI-DSI clock lane negative-end input pin. -If not used, please fix this pin at GND.	MCU
HSD0P	I/O	-MIPI-DSI data lane positive-end input pin. -If not used, please fix this pin at GND.	MCU
HSD0N	I/O	-MIPI-DSI data lane negative-end input pin. -If not used, please fix this pin at GND.	MCU
RDY	O	-Compressed processing busy flag is used to notice Host that compressed processing has completed. -If not used, please let this pin open.	OPEN

6.3 Driver Output Pins

Name	I/O	Description	Connect pin
S[840:1]	O	-Source output voltage signals applied to liquid crystal.	LCD
GOR[12:1] GOL[12:1]	O	-Gate control signals and the swing voltage level is VGH to VGL.	LCD
VGHO	O	-Power output (Positive) pin for gate driver.	LCD
VGLO	O	-Power output (Negative) pin for gate driver.	LCD
VGHO1	O	-Power output (Positive) pin for IGZO case. -Short VGHO for A-Si case	OPEN
VCOM	O	-A power supply for the TFT-LCD common electrode.	LCD
VCOM_OPT	O	-VCOM with Display scan , modulation signal with touch scan	LCD
CABCPWM	O	-PWM output signal to driving LED. -If not used, please let this pin open.	CABC

6.4 Touch Related Pin

Name	I/O	Description	Connect pin
TP_RESXP	I	-External reset for TP.	TP_RESXP
TP_OPT_1P	I	-Boot From Flash Pin , TP_OPT_1P ='0' : Host download. TP_OPT_1P ='1' : Flash Boot.	TP_OPT_1P
TP_OPT3P	I	-Touch test pin. -If not used, please let this pin GND.	TP_OPT3P
TP_UART_TX	O	-UART TX pad. -If not used, please let this pin open.	TP_UART_TX
TP_INT	O	-Touch screen interrupt. -If not used, please let this pin open.	TP_INT
TP_I2C_SCL	I/O	-I2C interface data pin. -If not used, please let this pin open.	TP_I2C_SCL
TP_I2C_SDA	I/O	-I2C interface clock pin. -If not used, please let this pin open.	TP_I2C_SDA
TP_SPI_MISO	O	-Slave input data pin in SPI interface. -If not used, please let this pin open.	TP_SPI_MISO
TP_SPI_MOSI	I	-Slave output data pin in SPI interface. -If not used, please let this pin VDDI or Open.	TP_SPI_MOSI
TP_SPI_SCL	I	-Slave clock pin in SPI interface. -If not used, please let this pin VDDI or Open.	TP_SPI_SCL
TP_SPI_CS	I	-Slave chip select pin in SPI interface. -If not used, please let this pin VDDI.	TP_SPI_CS
TP_FLASH_HOLD	I/O	- Master hold signal in SPI interface. -If not used, please let this pin open.	TP_FLASH_HOLD
TP_FLASH_WP	I/O	-Master write protect in SPI interface. -If not used, please let this pin open.	TP_FLASH_WP
TP_FLASH_CS	O	-Master chip select in SPI interface. -If not used, please let this pin open.	TP_FLASH_CS
TP_FLASH_MISO	I/O	-Master input data in SPI interface. -If not used, please let this pin open.	TP_FLASH_MISO
TP_FLASH_MOSI	I/O	-Master output data in SPI interface. -If not used, please let this pin open.	TP_FLASH_MOSI
TP_FLASH_SCL	O	-Master clock signal in SPI interface. -If not used, please let this pin open.	TP_FLASH_SCL
VAGP	O	-Modulation signal	VAGP

RX[210:1]	O	-TP Sensor Pins.	RX[210:1]

6.5 Test and Other Pins

Name	I/O	Description	Connect pin
TP_GPIO10~13	I/O	-Touch test pin. -Please leave it open	OPEN
EXTCLK_T	I	-Touch test pin. -If not used, please let this pin VDDI.	VDDI
EXTCLK_D	I	-Driver test pin. -If not used, please let this pin VDDI.	VDDI
TSTEN	I	-Driver test pin. -Please leave it open	OPEN
TSEL_0	I	-Driver test pin. -Please leave it open	OPEN
TSEL_1	I	-Driver test pin. -Please leave it open	OPEN
FRMP	I	-Driver test pin. -If not used, please let this pin GND.	GND
VGLI	O	-Used for monitoring -Please leave it open	OPEN
VCC	O	-Used for monitoring. -Please leave it open	OPEN
AVDD	O	-Power Pad for analog Circuit. -Please leave it open	OPEN
AVCL	O	-Power Pad for analog Circuit. -Please leave it open	OPEN
VAPP	O	-A power output of grayscale voltage. -Please leave it open	OPEN
VANP	O	-A power output (negative) of gray scale voltage. -Please leave it open	OPEN
VH	O	-Used for monitoring. -Please leave it open	OPEN
VTP	O	-Used for monitoring. -Please leave it open	OPEN
V20P	O	-Used for monitoring. -Please leave it open	OPEN

TEST[7:0]	O	-This pin is for testing -Please leave it open.	OPEN
DUMMY	-	-These pins are dummy. -Leave the pin open.	OPEN

7 DRIVER ELECTRICAL CHARACTERISTICS

7.1 Absolute Operation Range

Item	Symbol	Range	Unit
Supply Voltage (Analog)	VDD	- 0.3 ~ +4.6	V
Supply Voltage (I/O)	VDDI	- 0.3 ~ +4.6	V
Supply Voltage (Logic)	VCC	-0.3 ~ +2	V
Driver Supply Voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic Input Voltage Range	VIN	0.5 ~ VDDI + 0.5	V
Logic Output Voltage Range	VO	0.5 ~ VDDI + 0.5	V
Operating Temperature Range	TOPR	-30 ~ +85	℃
Storage Temperature Range	TSTG	-40 ~ +125	℃

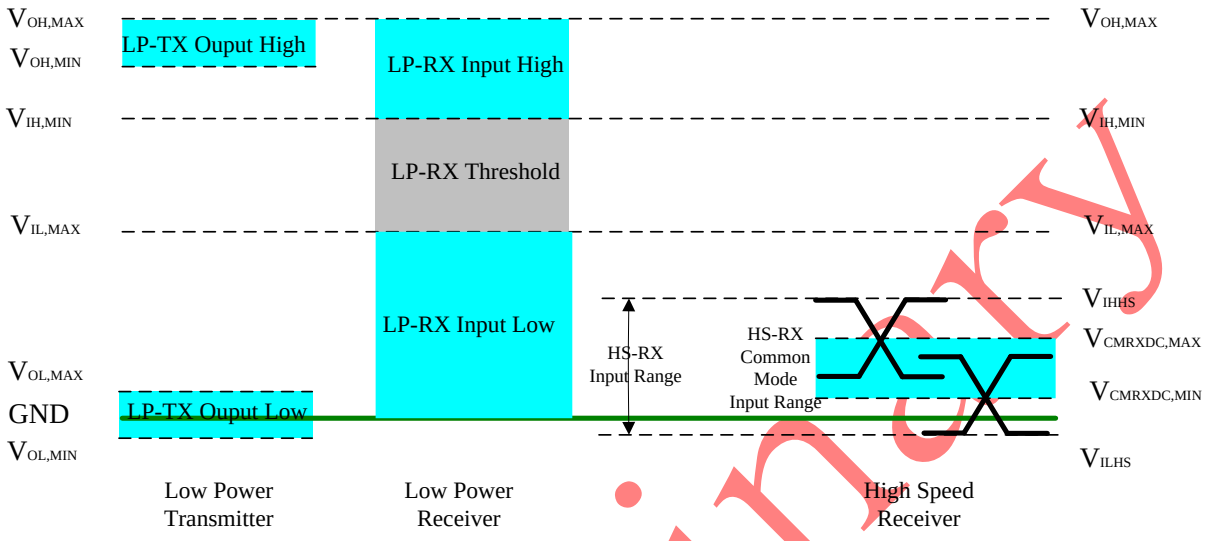
Absolute Operation Range

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

7.2 DC Characteristics

7.2.1 DC characteristics for MIPI DSI

● MIPI Signaling Voltage Levels



● MIPI DC characteristics

Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Operation Voltage for MIPI Receiver					
Low power mode operating voltage	V_{LPH}	1.1	1.2	1.3	V
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Common-mode voltage	V_{CMRXDC}	70	-	330	mV
Differential input impedance	Z_{ID}	80	100	125	ohm
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	V_I	-50	-	1350	mV
Logic 0 input threshold	V_{IL}	0	-	550	mV
Logic 1 input threshold	V_{IH}	880	-	1350	mV
Output low level	V_{OL}	-50	-	50	mV
Output high level	V_{OH}	1.1	1.2	1.3	V

7.2.2 DC characteristics for Panel Driving

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			MIN.	TYP.	MAX.		
Power & Operation Voltage							
System Voltage	VDD	Operating voltage	2.65	2.8	3.3	V	-
Interface Operation Voltage	VDDI	I/O Supply Voltage	1.65	1.8	3.3	V	-
Gate Driver High Voltage	VGH	-	7.5	-	15.5	V	-
Gate Driver Low Voltage	VGL	-	-12	-	-6.5	V	-
Gate Driver Supply Voltage	-	| VGH-VGL |	-	-	27.5	V	-
Input / Output							
Logic-High Input Voltage	VIH	-	0.7VDDI	-	VDDI	V	Note 1
Logic-Low Input Voltage	VIL	-	GND	-	0.3VDDI	V	Note 1
Logic-High Output Voltage	VOH	IOH = -1.0mA	0.8VDDI	-	VDDI	V	Note 1
Logic-Low Output Voltage	VOL	IOL = +1.0mA	GND	-	0.2VDDI	V	Note 1
Logic-High Input Current	IIH	VIN = VDDI	-	-	1	uA	Note 1
Logic-Low Input Current	IIL	VIN = GND	-1	-	-	uA	Note 1
Input Leakage Current	ILI	IOH = -1.0mA	-0.1	-	+0.1	uA	Note 1
VCOM Voltage							
VCOM Voltage	VCOM	-	-	GND	-	V	-
Source Driver							
Gamma Reference Voltage(Positive)	VAP	-	3.8	-	6.4	V	-
Gamma Reference Voltage(Negative)	VAN	-	-4.4	-	-2	V	-
Source Output Settling Time	Tr	Below with 99% precision	-	-	20	us	Note 2

Basic DC Characteristics

Notes:

1. TA= -30 to 85℃.

2. The max. value is between measured point of source output and gamma setting value.

7.3 Power Consumption

Ta=25℃, Frame rate = 60Hz, Registers setting are IC default setting.

Operation Mode	Image	Current Consumption			
		Typical		Maximum	
		IDDI (mA)	IDD (mA)	IDDI (mA)	IDD (mA)
Normal Mode	Note	TBD	TBD	TBD	TBD
Sleep-in Mode	Note	TBD	TBD	TBD	TBD
Deep Standby Mode	Note	TBD	TBD	TBD	TBD

Notes:

1. Color Picture.

2. The Current Consumption is DC characteristics of ST77922.

3. Typical: VDDI=1.8V, VDD=2.8V; Maximum: VDDI=3.3V, VDD=3.3V

7.4 AC Characteristics

7.4.1 8080 Series MCU Parallel Interface Characteristics: 8-bit Bus

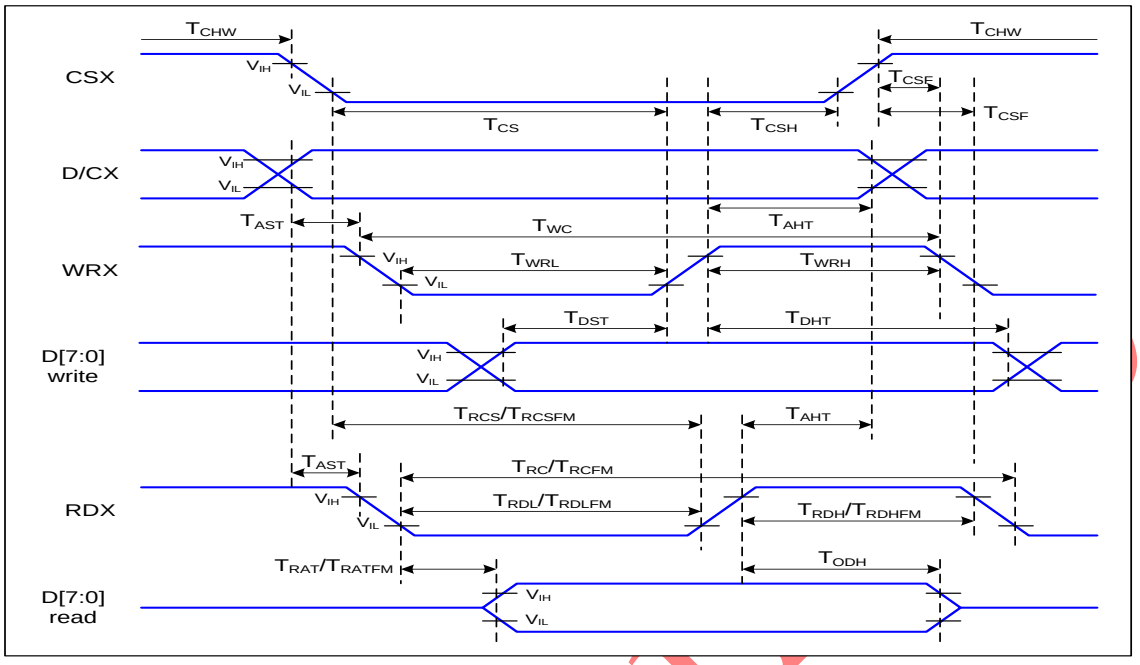


Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.65 to 3.3V, VDD=2.65 to 3.3V, GND=RGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select “H” pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	26		ns	
	T_{WRH}	Control pulse “H” duration	13		ns	
	T_{WRL}	Control pulse “L” duration	13		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse “H” duration (ID)	90		ns	
	T_{RDL}	Control pulse “L” duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse “H” duration (FM)	90		ns	

	T_{RDLFM}	Control pulse “L” duration (FM)	355		ns	
D[7:0]	T_{DST}	Data setup time	10		ns	For CL=30pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)		40	ns	
	T_{RATFM}	Read access time (FM)		340	ns	
	T_{ODH}	Output disable time	20	80	ns	

Table 1 8080 Parallel Interface Characteristics

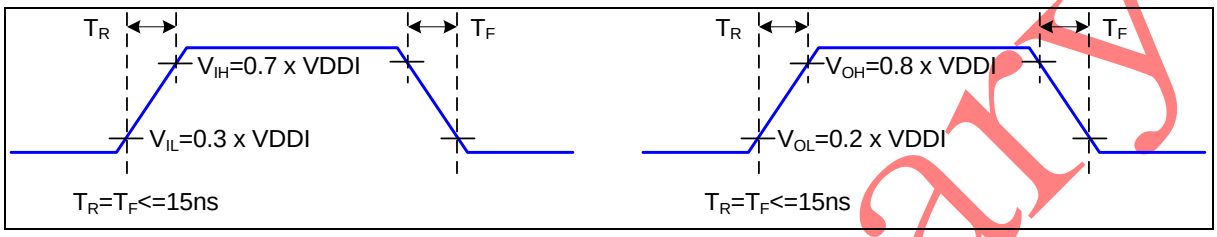


Figure 2 Rising and Falling Timing for I/O Signal

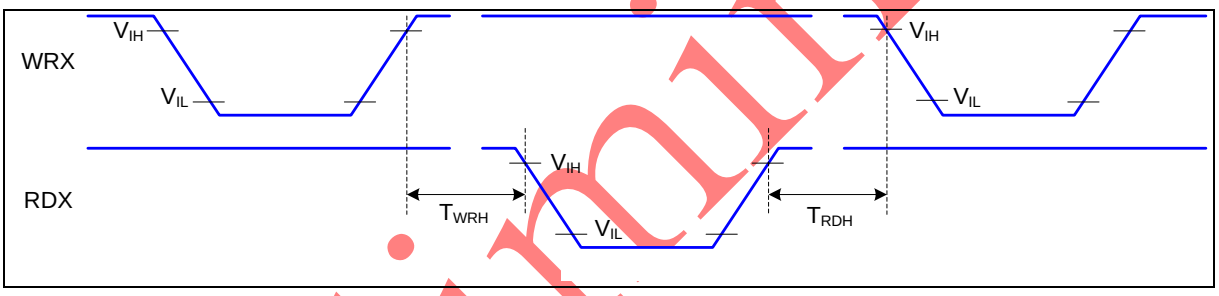


Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.4.2 Serial Interface Characteristics (3-line serial):

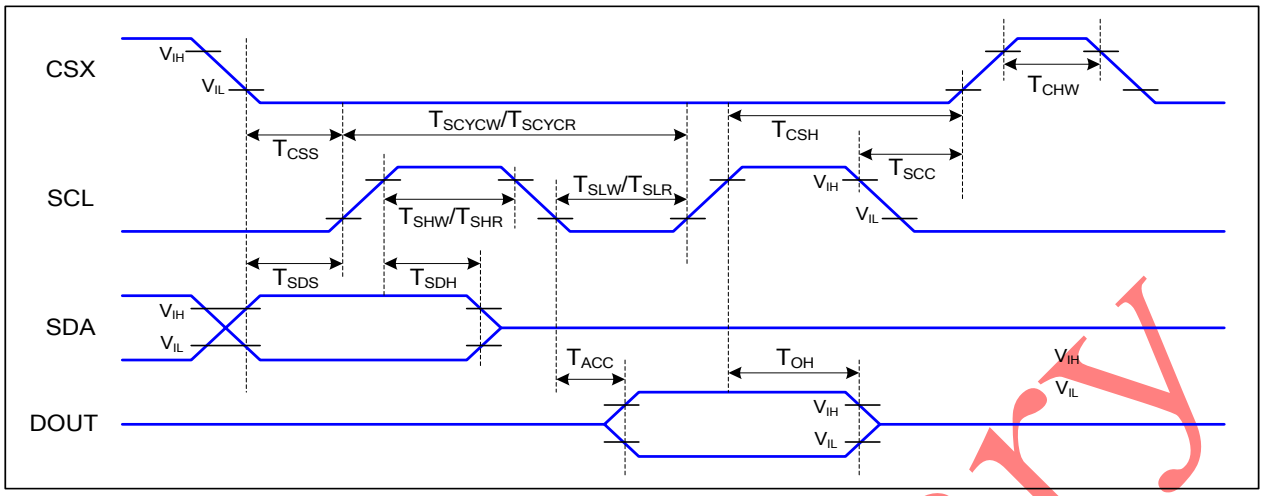


Figure 4 3-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.65 to 3.3V, GND=RGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	
	T_{SHW}	SCL “H” pulse width (Write)	7		ns	
	T_{SLW}	SCL “L” pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	7		ns	
	T_{SDH}	Data hold time	7		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 2 3-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.4.3 Serial Interface Characteristics (4-line serial):

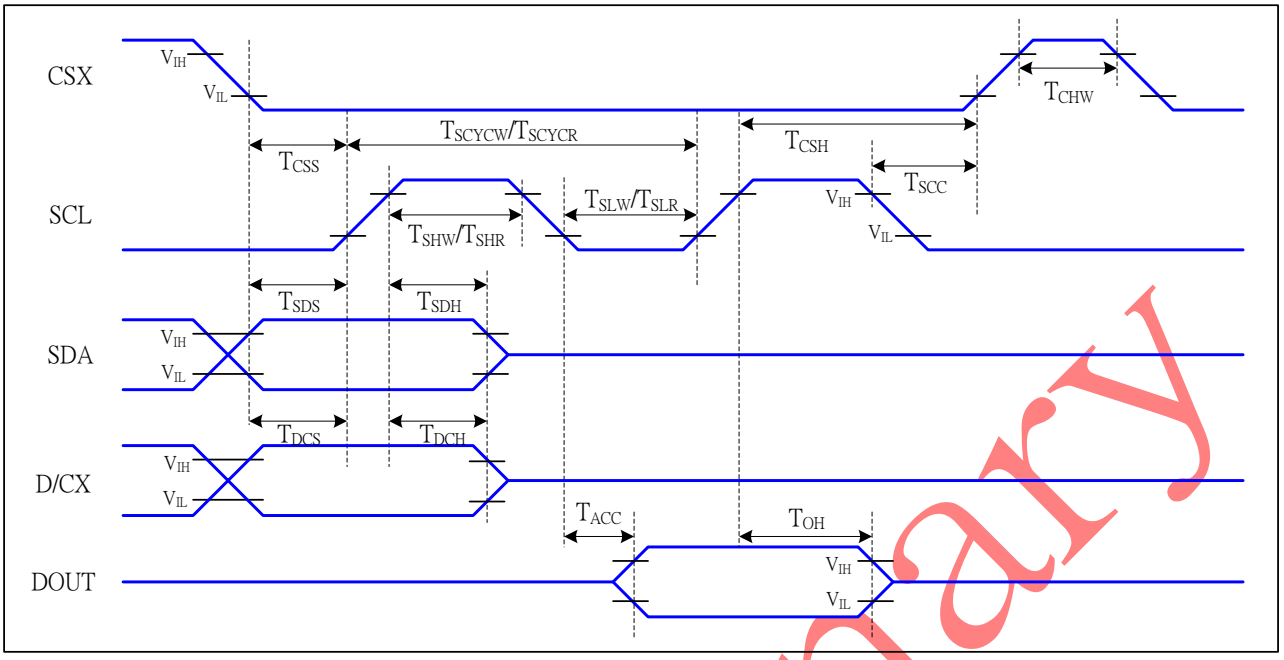


Figure 5 4-line serial Interface Timing Characteristics

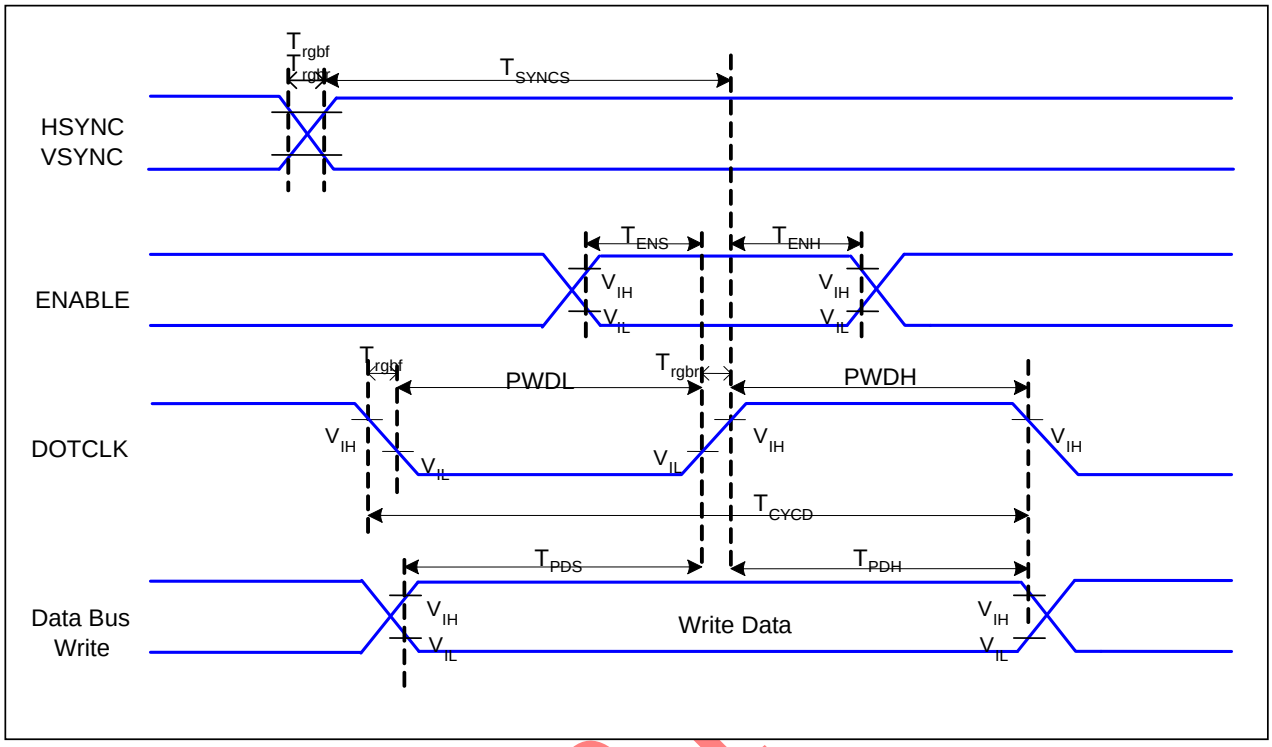
VDDI=1.65 to 3.3V, VDD=2.65 to 3.3V, GND=RGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	-write command & data ram
	T_{SHW}	SCL “H” pulse width (Write)	7		ns	
	T_{SLW}	SCL “L” pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	7		ns	
	T_{SDH}	Data hold time	7		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 3 4-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.4.4 RGB Interface Characteristics:



VDDI=1.65 to 3.3V, VDD=2.65 to 3.3V, GND=RGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	15	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	15	-	ns	
	T_{ENH}	Enable Hold Time	15	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	15	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	15	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	30	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	10	ns	
DB	T_{PDS}	PD Data Setup Time	15	-	ns	
	T_{PDH}	PD Data Hold Time	15	-	ns	

Table 4 6 Bits RGB Interface Timing Characteristics

7.4.5 QSPI Interface Characteristics:

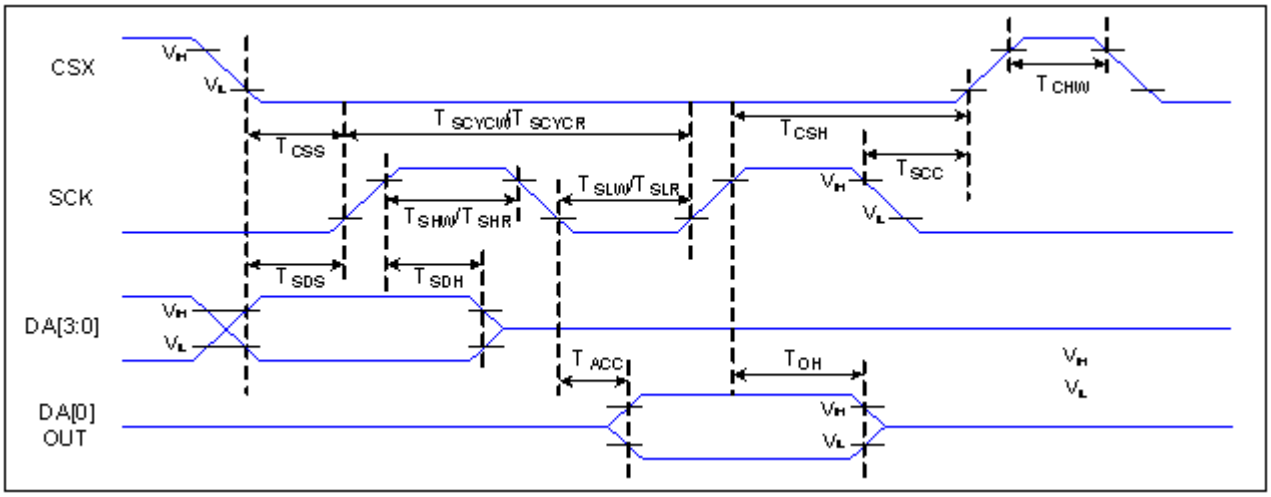


Figure 7 QSPI Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.65 to 3.3V, GND=RGND=0V, Ta=25℃

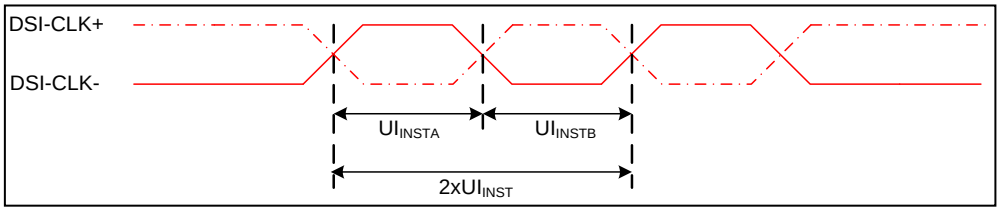
Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	19		ns	
	T_{CSH}	Chip select hold time (write)	19		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
			200		ns	*Note1*
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	
	T_{SHW}	SCL “H” pulse width (Write)	7		ns	
	T_{SLW}	SCL “L” pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	7		ns	
	T_{SDH}	Data hold time	7		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	TBD	TBD	ns	For minimum CL=8pF

Table 5 QSPI Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

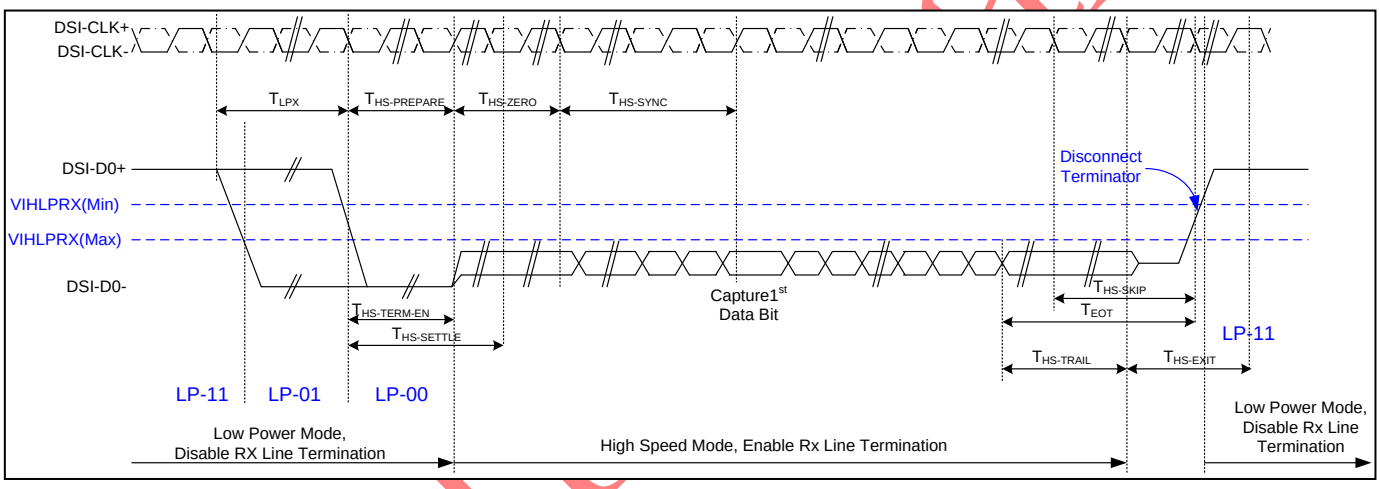
7.4.6 MIPI Interface Characteristics

High Speed Mode – Clock Channel Timing



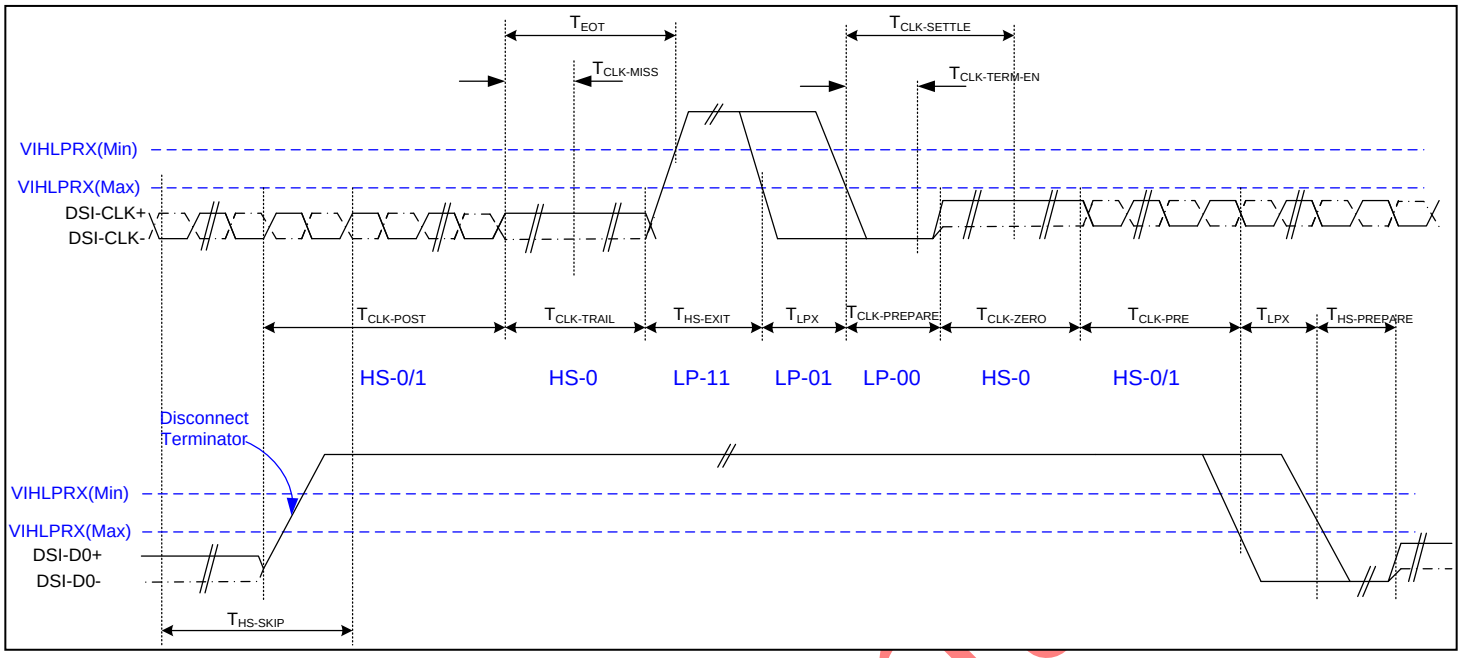
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-DATA_P/N	2xUI INST	Double UI instantaneous	2.66	25	ns	
DSI-DATA_P/N	UI INSTA ,UI INSTB	UI instantaneous Half	1.33	12.5	ns	

High-Speed Data Transmission



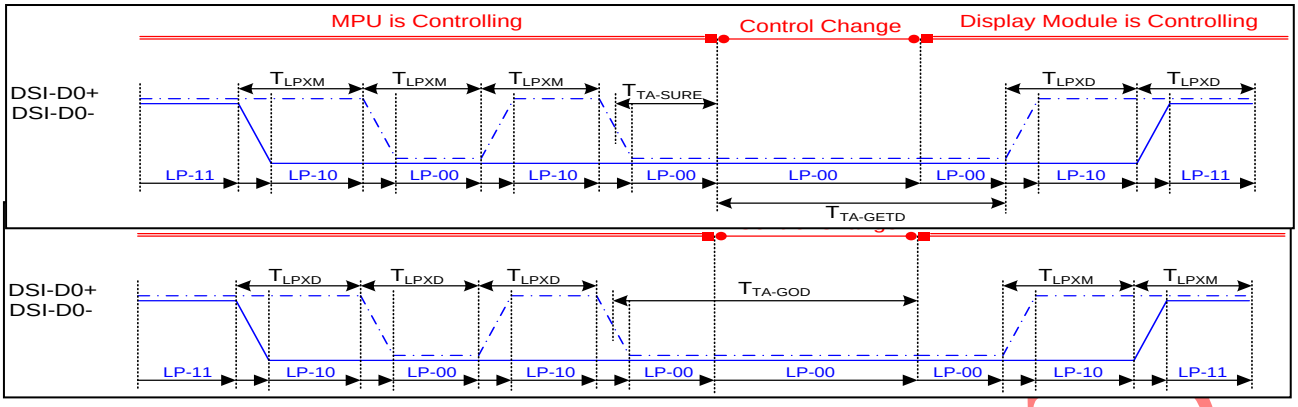
Parameter	Symbol	MIN	TYP	MAX	Unit
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI		85+6UI	ns
Time from start of t HS-TRAIL or t CLK-TRAIL period to start of LP-11 state	T_{EOT}			105+12UI	ns
Time to enable data receiver line termination measured from when Dn crosses VILMAX	$T_{HS-TERM-EN}$			35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission	$T_{HS-TRAIL}$	60+4UI			ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40		55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100			ns
Length of any Low-Power state period	T_{LPX}	50			ns
Sync sequence period	$T_{HS-SYNC}$		8UI		ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI			ns

Switching the Clock Lane between Clock Transmission and Low-Power Mode



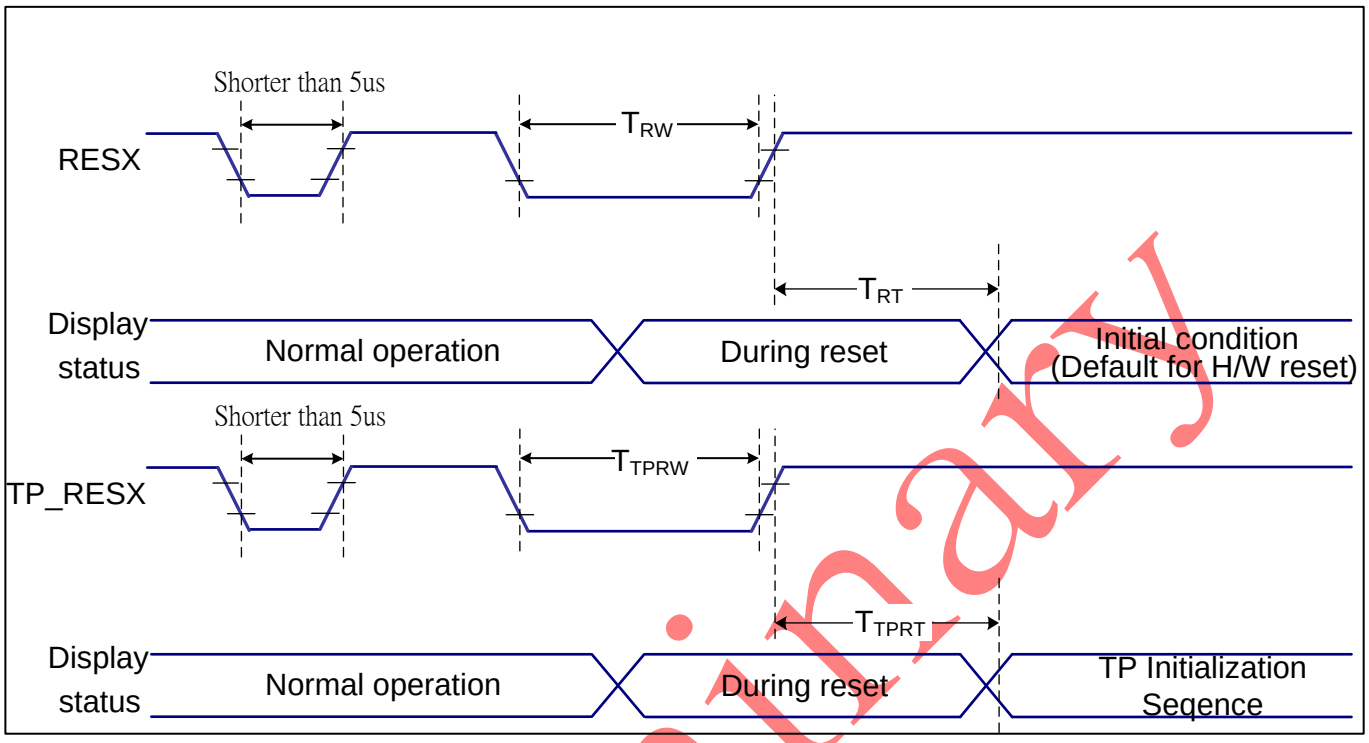
Parameter	Symbol	MIN	TYP	MAX	Unit
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52UI			ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$			60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38		95	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	300			ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$			38	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8			UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60			ns

Bus Turnaround Procedure



Parameter	Symbol	MIN	TYP	MAX	Unit
Length of any Low-Power state period : Master side	T_{LPX}	50		75	ns
Length of any Low-Power state period : Slave side	T_{LPX}	47.5	50	52.5	ns
Ratio of T_{LPX} (MASTER)/ T_{LPX} (SLAVE) between Master and Slave side	Ratio T_{LPX}	2/3		3/2	
Time-out before new TX side start driving	$T_{TA-SURE}$	T_{LPX}		2 T_{LPX}	ns
Time to drive LP-00 by new TX	T_{TA-GET}		5 T_{LPX}		Ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		4 T_{LPX}		ns

7.4.7 Reset Timing



VDDI=1.8V,VDD=2.8V, GND=0V, Ta=25℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
			-	120 (Note 1, 6, 7)	ms
TP_RESX	TTPRW	Reset pulse duration	10	-	us
	TTPRT	Reset cancel	-	100	ms

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

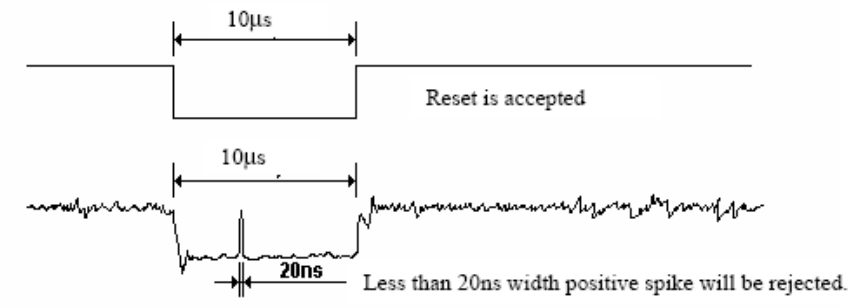
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120

ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:

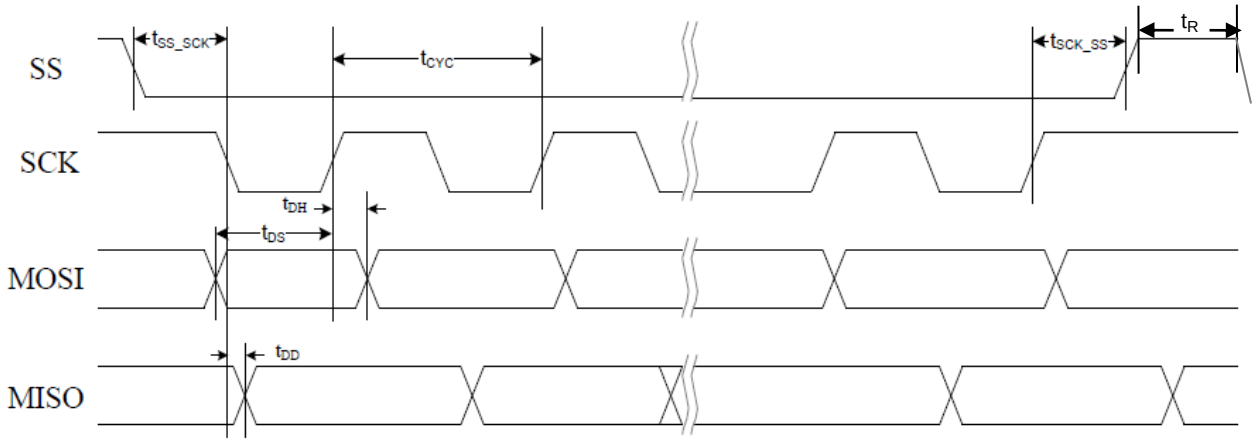


5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

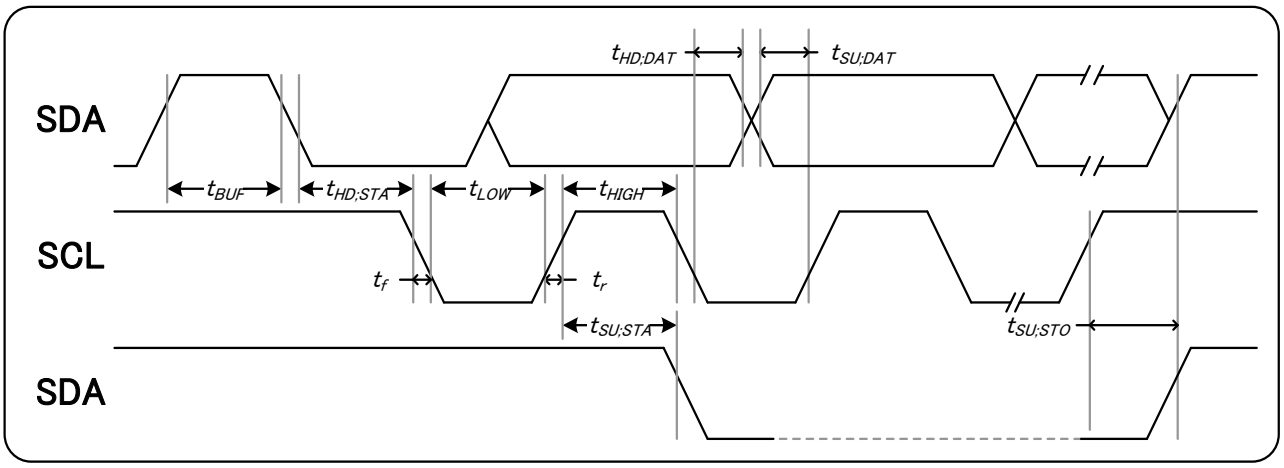
7.4.8 Touch SPI Timing



VDDI=1.8V,VDD=2.8V, GND=0V, Ta=25℃

Symbol	Parameter	Rating			Unit
		Min.	Typ.	Max.	
f_{SCK}	SCK frequency	-	-	12	Mhz
t_{CYC}	SCK cycle time	125	-	-	ns
t_{DS}	Data setup time prior SCK rising	25	-	-	ns
t_{DH}	Data hold time after SCK rising	25	-	-	ns
t_{DD}	MISO data output delay from SCK falling	-	-	50	ns
t_{SS_SCK}	SS falling to 1st SCK falling	1000	-	-	ns
t_{SCK_SS}	SCK rising to SS rising	1000	-	-	ns
t_R	CS recovery time	28	-	-	us

7.4.9 Touch I2C Timing



VDDI=1.8V,VDD=2.8V, GND=0V, Ta=25℃

Item	Signal	Symbol	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	SCL	f_{SCL}			400	khz
SCL clock low period		t_{LOW}	1250			ns
SCL clock high period		t_{HIGH}	1250			ns
Data set-up time	SDA	$t_{SU;DAT}$	100			ns
Data hold time		$t_{HD;DAT}$	0			ns
Setup time for a repeated START condition	SDA	$t_{SU;STA}$	600			ns
Start condition hold time		$t_{HD;STA}$	600			ns
Setup time for STOP condition		$t_{SU;STO}$	600			ns
Bus free time between a STOP and START		t_{BUF}	1300			ns

8 INTERFACE

8.1 MPU Interface Type Selection

ST77922 supports 8 bit parallel data bus for 8080 series CPU, RGB serial interfaces, SPI interface, QSPI interface, MIPI interface. Selection of these interfaces are set by IM[2:0] pins as shown below.

IM2	IM1	IM0	MPU Interface Mode	Data pin
0	0	0	3-line 9bit serial I/F	SDA: in/out
0	0	1	4-line 8bit serial I/F	SDA: in/out
0	1	0	2 data lane serial I/F	SDA0: in/out、SDA1: in
0	1	1	QSPI I/F	SDA[3:0]: in/out
1	0	0	RGB_3-line 9bit serial I/F	SDA: in/out、DB[7:0]
1	0	1	RGB_4-line 8bit serial I/F	SDA: in/out、DB[7:0]
1	1	0	MIPI I/F	DP/DN
1	1	1	80-8bit parallel I/F	DB[7:0]

Table 6 Interface Type Selection

8.2 8080-Ⅰ Series MCU Parallel Interface

The MCU can use 8080-8bits parallel interface: 11-lines with 8-data parallel interface. The chip-select CSX (active low) enables/disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write enable, RDX is the parallel data read enable and D[7:0] is parallel data bus.

The LCD driver reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[7:0] bits is either display data or command parameter. When D/C='0', D[7:0] bits is command. The interface functions of 8080-8bits parallel interface are given in following table.

IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Read back selection
1	1	1	8-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
				1	1	↑	Write 8-bit display data or 8-bit parameter (D7 to D0)
				1	↑	1	Read 8-bit display data (D7 to D0)
				1	↑	1	Read 8-bit parameter or status (D7 to D0)

Table 7 the function of 8080 - 8 bits parallel interface

8.2.1 Write cycle sequence

The write cycle means that the host writes information (command / data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control signals (DCX, RDX, WRX) and data signals (DB[7:0]). DCX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (=’0’) and vice versa it is data (=’1’).

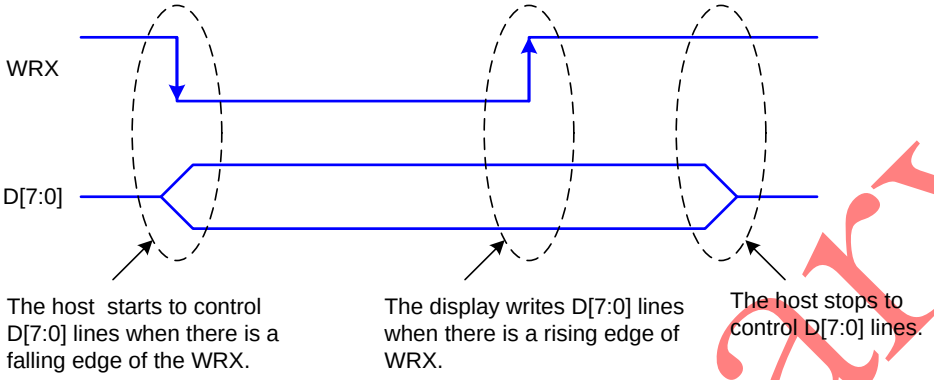


Figure 8 8080 - 8 bits WRX Protocol

Note: WRX is an unsynchronized signal (It can be stopped).

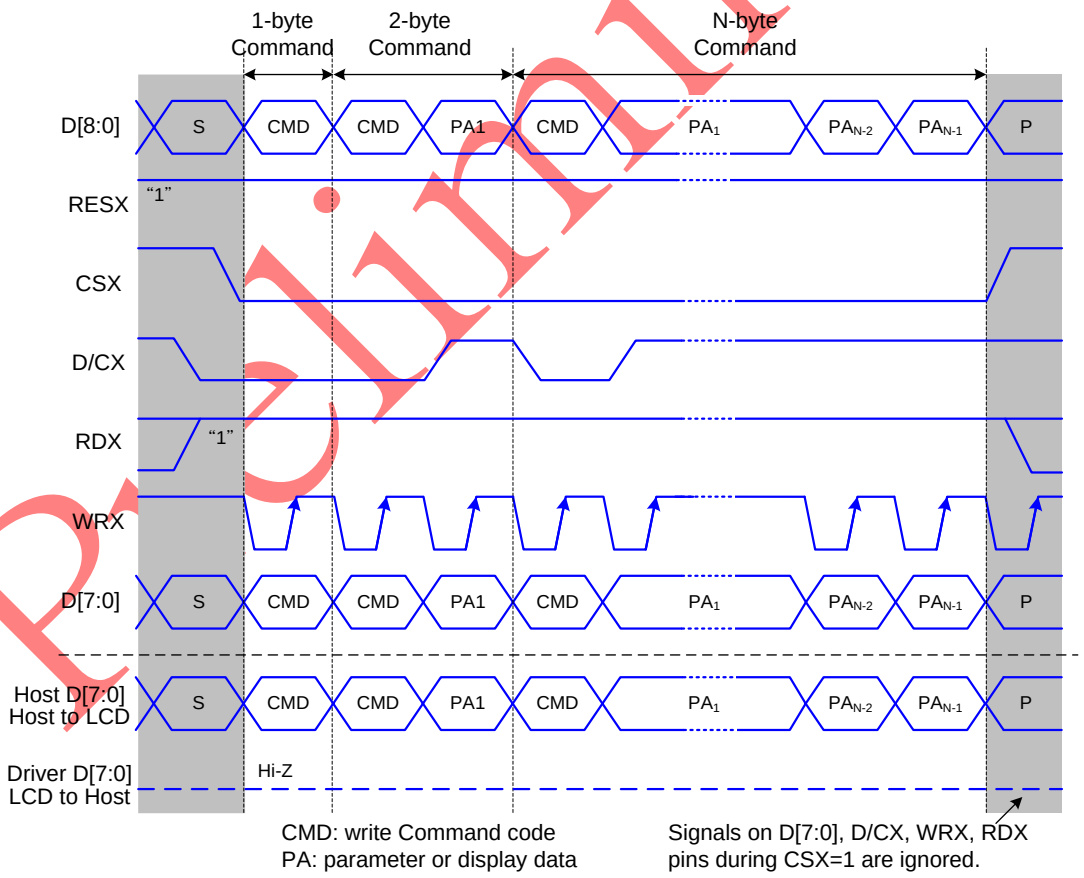


Figure 9 8080 - 8 bits Parallel Bus Protocol, Write to Register or Display RAM

8.2.2 Read cycle sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from LCD driver via interface. The driver sends data (D[7:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

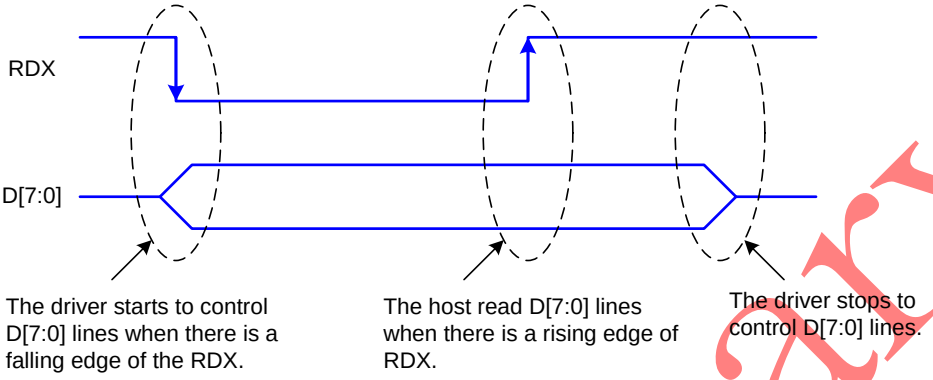


Figure 10 8080 – 8 bits RDX protocol

Note: RDX is an unsynchronized signal (It can be stopped).

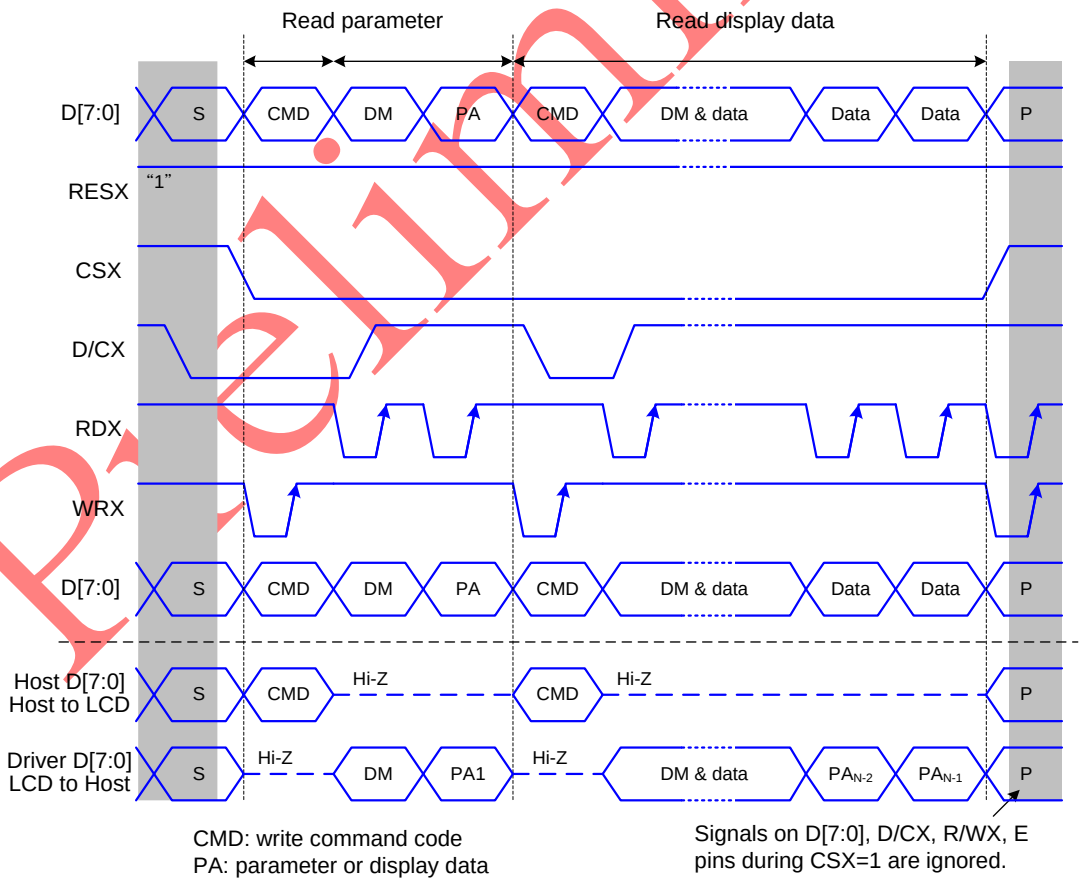


Figure 11 8080 - 8 bits parallel bus protocol, read data from register or display RAM

8.3 Serial Interface

IM2	IM1	IM0	Interface	Read back selection
0	0	0	3-line serial interface Ⅰ	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
0	0	1	4-line serial interface Ⅰ	

Table 8 Selection of serial interface

The serial interface is either 3-lines/9-bits or 4-lines/8-bits bi-directional interface for communication between the micro controller and the LCD driver. The 3-lines serial interface use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output), and the 4-lines serial interface use: CSX (chip enable), D/CX (data/ command flag), SCL (serial clock) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

8.3.1 Pin description

3-line serial interface Ⅰ

Pin Name	Description
CSXP	Chip selection signal
RDXP (SCL)	Clock signal
SDA	Serial input/output data

4-line serial interface Ⅰ

Pin Name	Description
CSXP	Chip selection signal
DCXP (A0)	Data is regarded as a command when DCXP is low Data is regarded as a parameter or data when DCXP is high
RDXP (SCL)	Clock signal
SDA	Serial input/output data

Table 9 pin description of serial interface

8.3.2 Command write mode

The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-lines serial data packet contains a control bit D/CX and a transmission byte. In 4-lines serial interface, data packet contains just transmission byte and control bit D/CX is transferred by the D/CX pin. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is stored in the display data RAM (memory write command), or command register as parameter.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

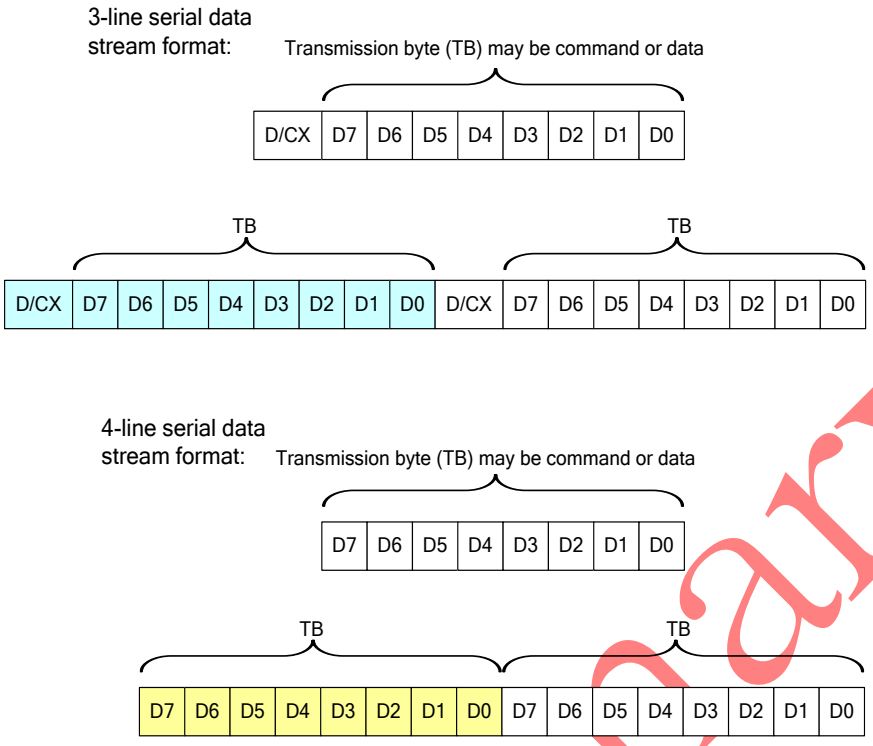


Figure 12 Serial interface data stream format

When CSX is “high”, SCL clock is ignored. During the high period of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low. SDA is sampled at the rising edge of SCL. D/CX indicates whether the byte is command (D/CX=’0’) or parameter/RAM data (D/CX=’1’). D/CX is sampled when first rising edge of SCL (3-line serial interface) or 8th rising edge of SCL (4-line serial interface). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-line serial interface) or D7 (4-line serial interface) of the next byte at the next rising edge of SCL..

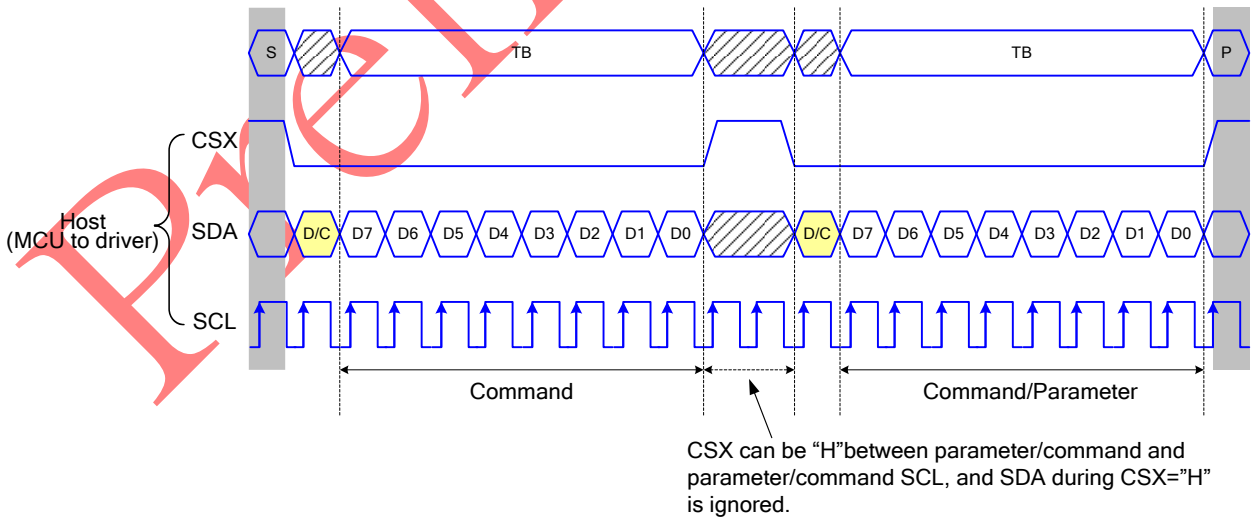


Figure 13 3-line serial interface write protocol (write to register with control bit in transmission)

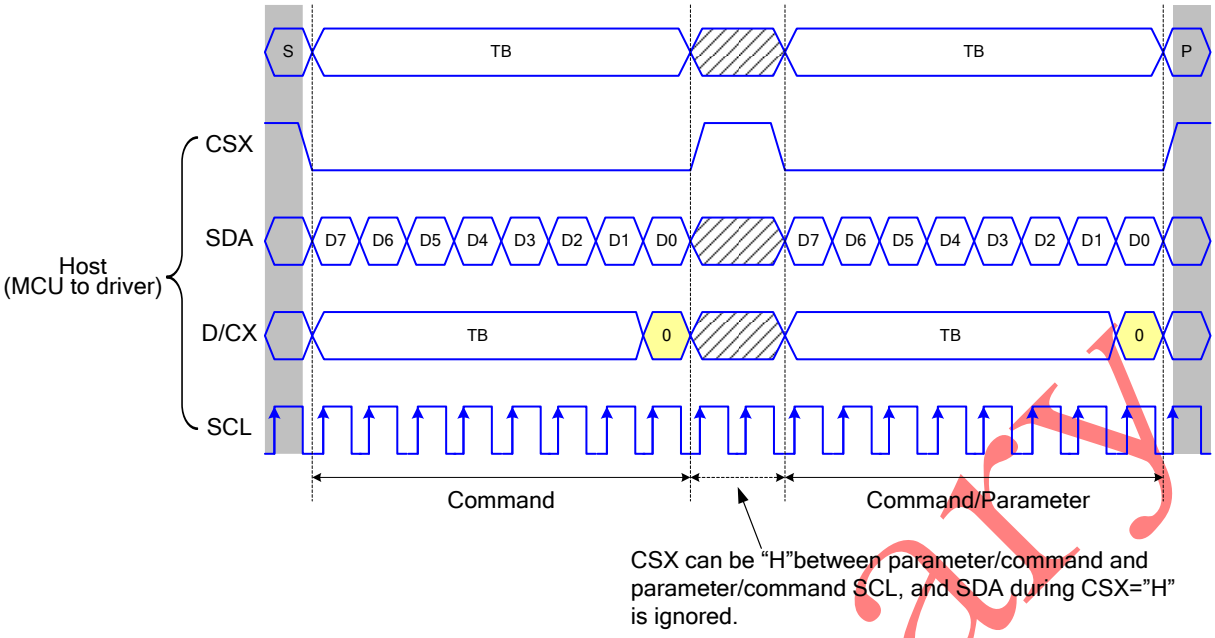


Figure 14 4-line serial interface write protocol (write to register with control bit in transmission)

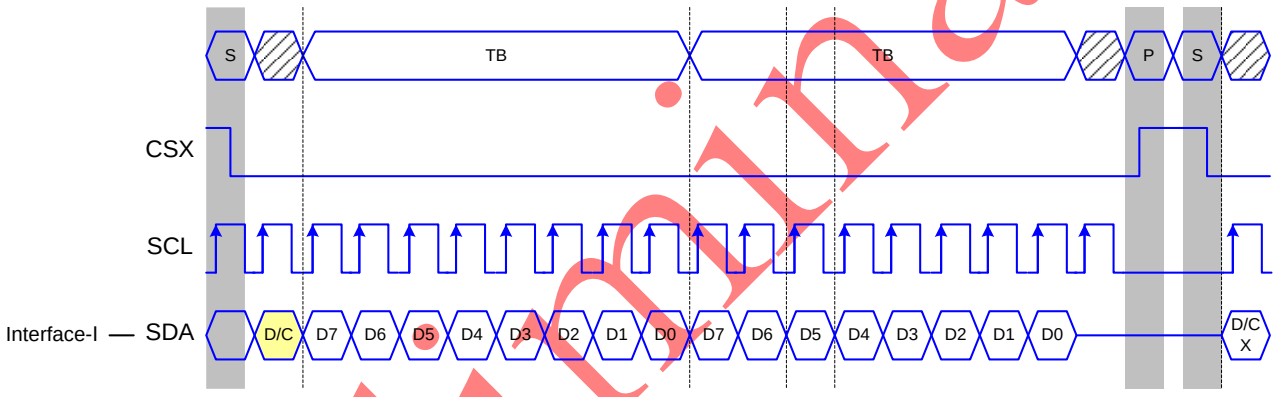
8.3.3 Read function

The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

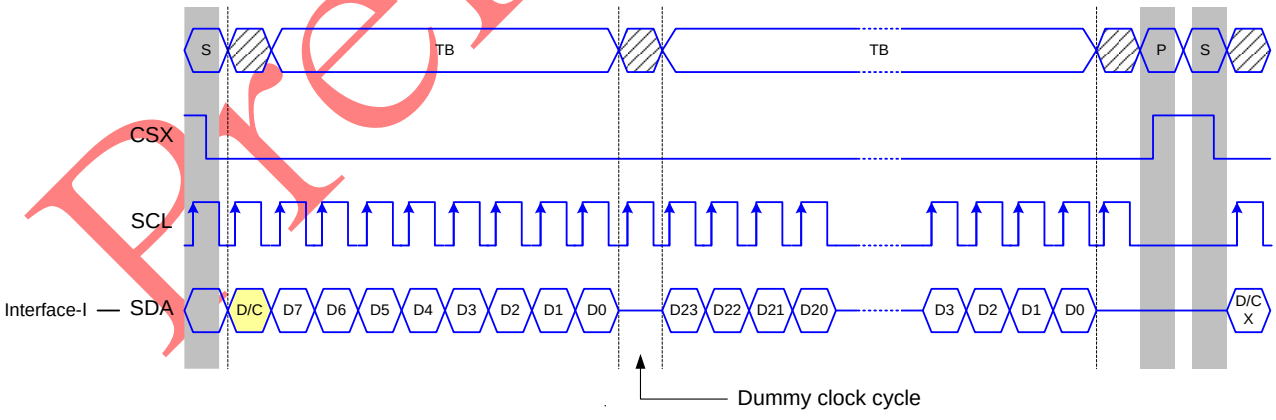
After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

8.3.4 3-line serial interface Ⅰ protocol

3-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



3-line serial protocol (for RDDID command: 24-bit read):



3-line Serial Protocol (for RDDST command: 32-bit read):

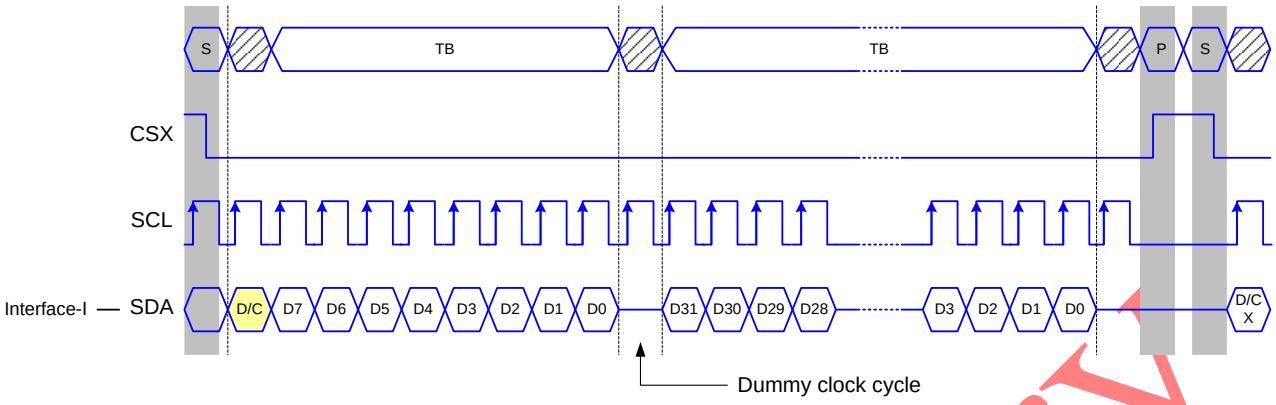
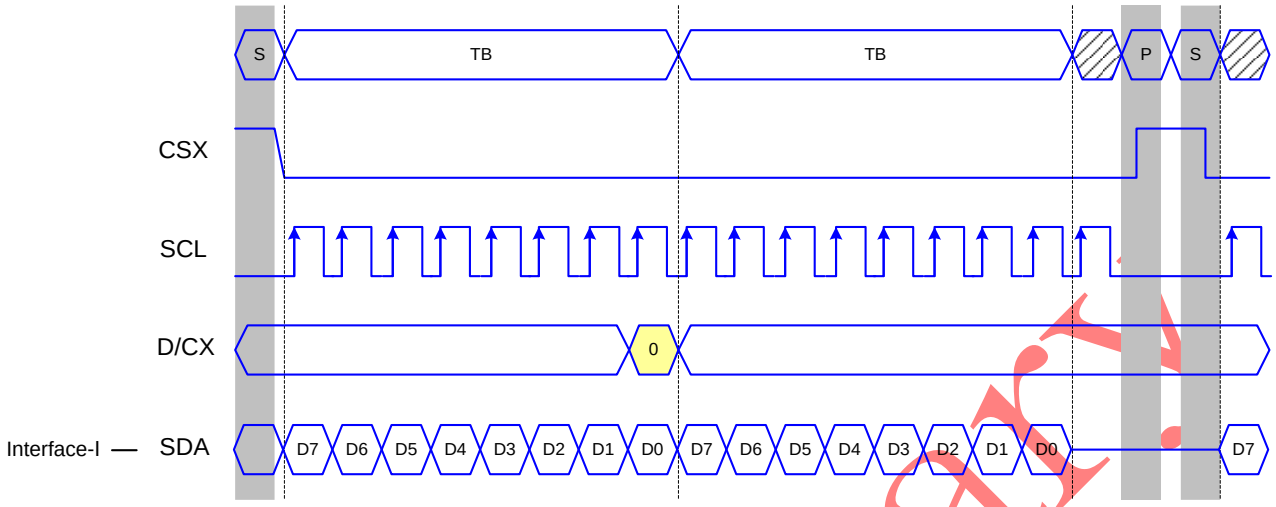


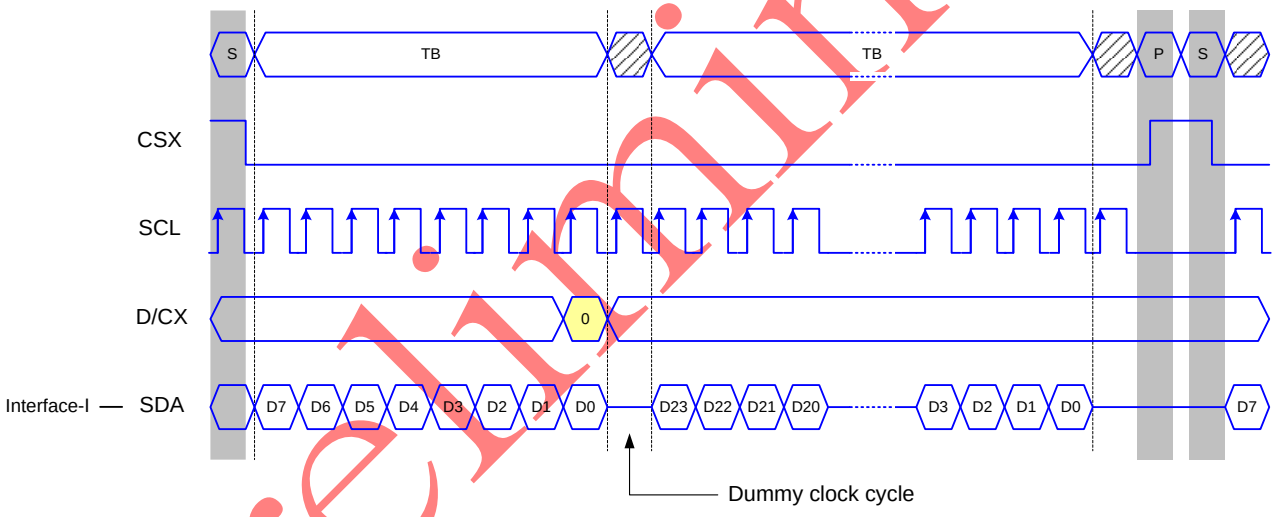
Figure 15 3-line serial interface read protocol

8.3.5 4-line serial protocol

4-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



4-line serial protocol (for RDDID command: 24-bit read)



4-line Serial Protocol (for RDDST command: 32-bit read)

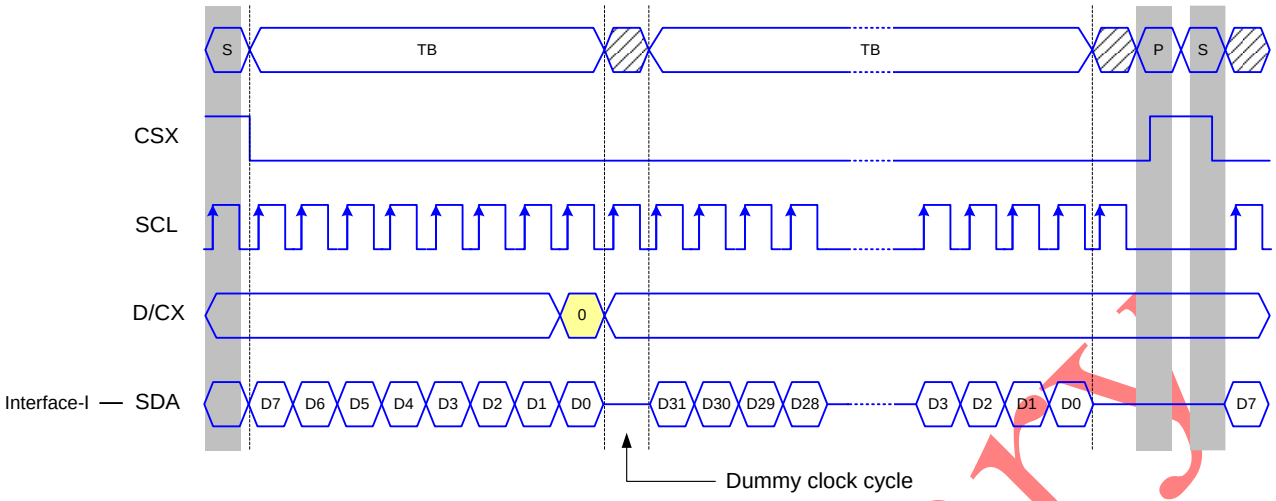


Figure 16 4-line serial interface read protocol

8.4 2 data lane serial Interface

Interface selection:

IM2	IM1	IM0	Interface	Read back selection
0	1	0	2 data lane serial interface	Via the read instruction (8-bit, 24-bit and 32-bit read)

Table 10 IM pin selection

2-wire data lane serial interface use: CSX (chip enable), SCL (serial clock) and SDA1 (serial data input/output 1), and SDA2 (serial data input 2).

2 data lane hardware suggestion and Pin description:

2 data lane serial interface, IM[2:0]=010

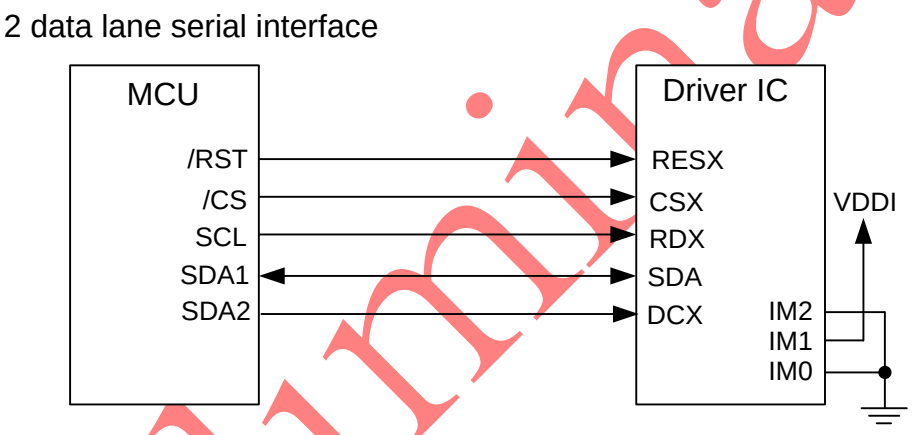


Figure 17 Hardware suggestion of 2 data lane serial interface

Pin Name	Description
CSX	Chip selection signal
RDX (SCL)	Clock signal
SDA (SDA1)	Serial data input/output1
DCX(SDA2)	Serial data input2

Table 11 Pin description of 2 data lane serial interface

Command write mode:

The command write protocol of 2-wire data lane serial interface is the same with the 3-line serial interface, so users can ignore the input data of DCX.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

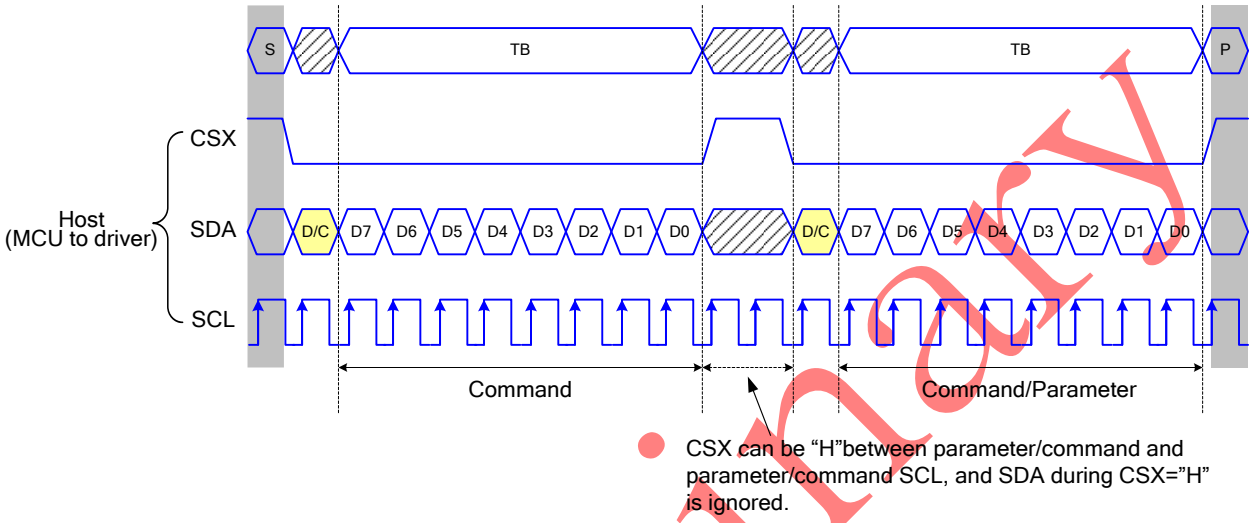


Figure 18 3-line serial interface write protocol (write to register with control bit in transmission)

SRAM write mode:

The SRAM write mode of 2-wire data line serial interface need use SDA pin and DCXP pin to be data input pins.

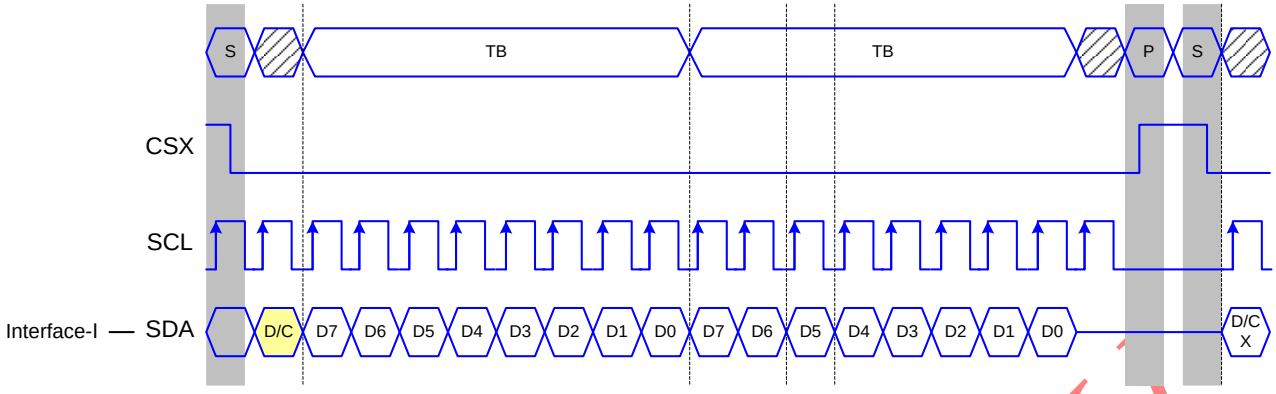
Read function:

The read mode of 2-wire data lane serial interface is the same with the 3-line serial interface and DCXP pin can be ignored. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

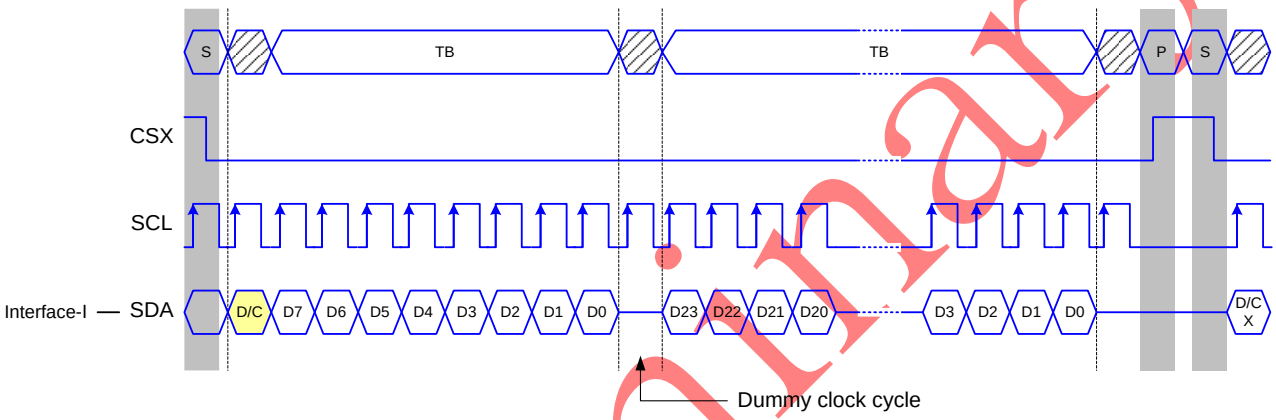
After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

3-line serial interface Ⅰ protocol:

3-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



3-line serial protocol (for RDDID command: 24-bit read)



3-line Serial Protocol (for RDDST command: 32-bit read)

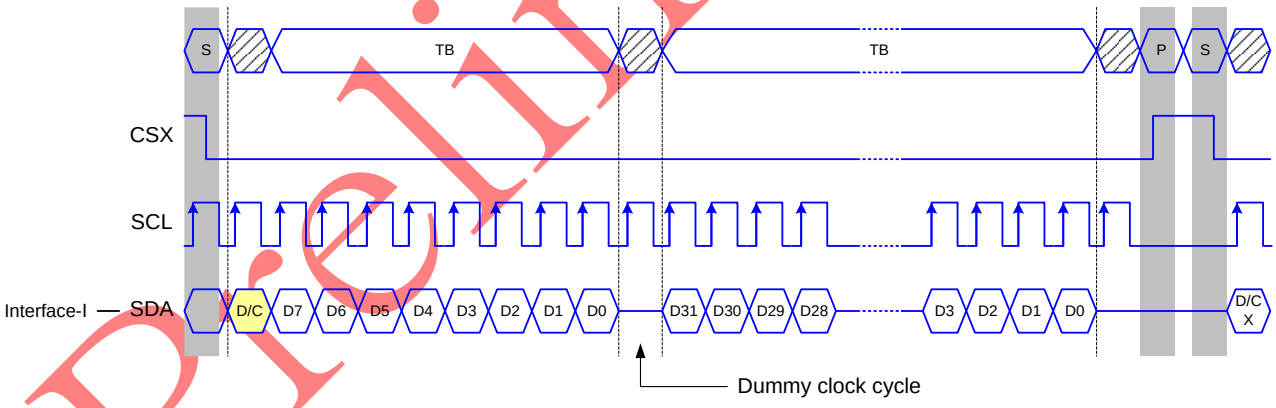


Figure 19 3-line serial interface read protocol

8.5 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been HIGH state.

If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated.

If 1, 2 or more parameter commands are being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

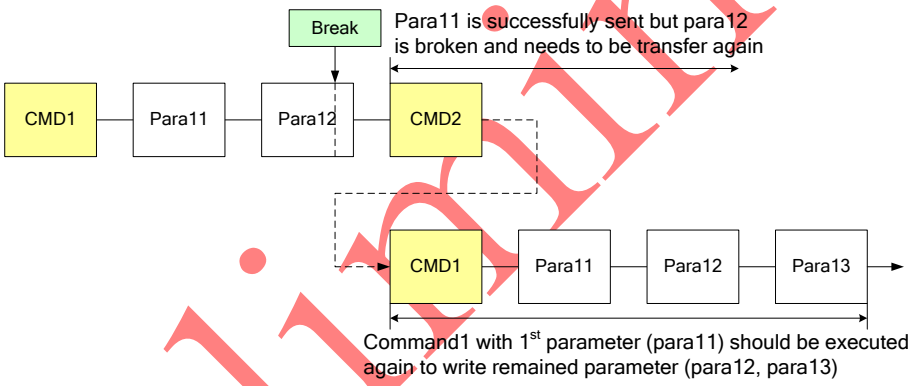


Figure 20 Write interrupts recovery (serial interface)

If a 2 or more parameter commands are being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

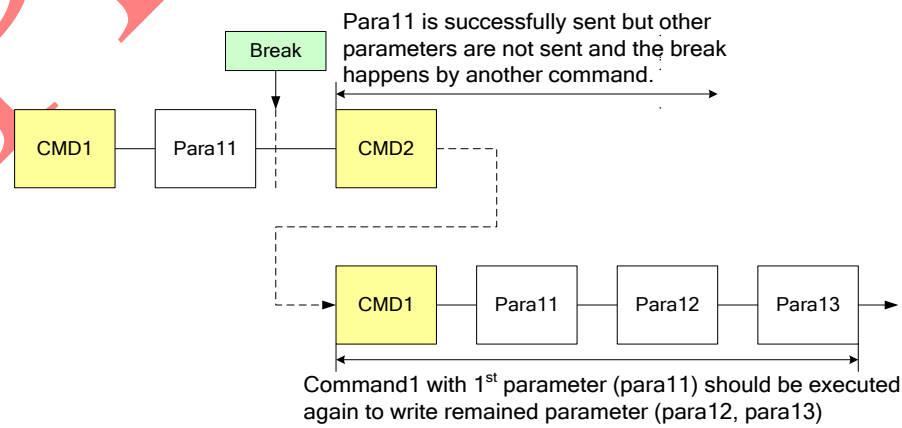


Figure 21 Write interrupts recovery (both serial and parallel Interface)

8.6 Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the Chip Select line is released after a whole byte of a frame memory data or multiple parameter data has been completed, then driver will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the Chip Select line is released after a whole byte of a command has been completed, then the display module will receive either the command‘s parameters (if appropriate) or a new command when the Chip Select line is next enabled as shown below.

This applies to the following 4 conditions:

1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

8.6.1 Parallel interface pause

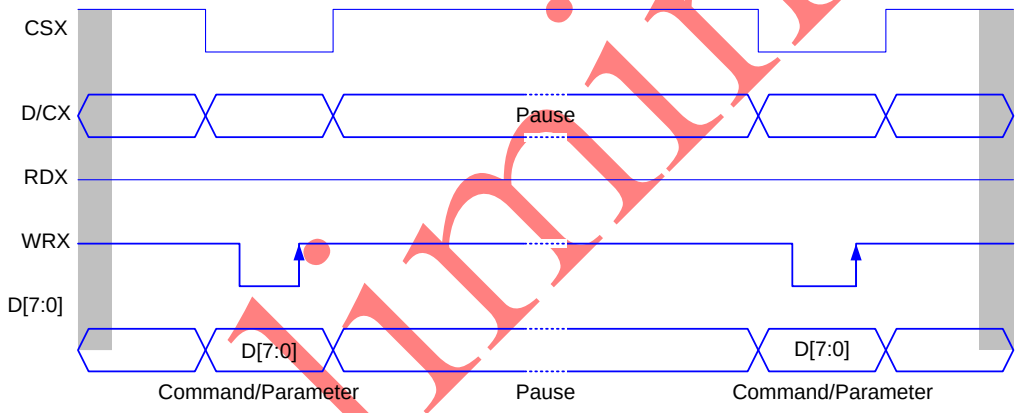


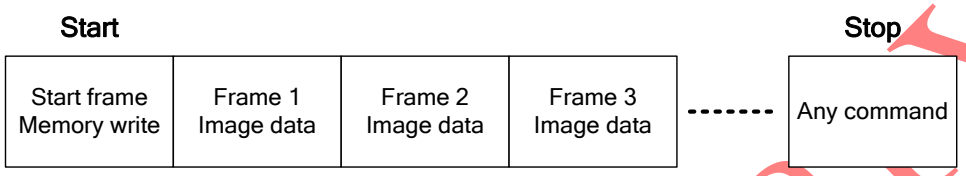
Figure 22 Parallel bus pause protocol (paused by CSX)

8.7 Data Transfer Mode

The module has two kinds color modes for transferring data to the display RAM. These are 16-bit color per pixel and 18-bit color per pixel. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

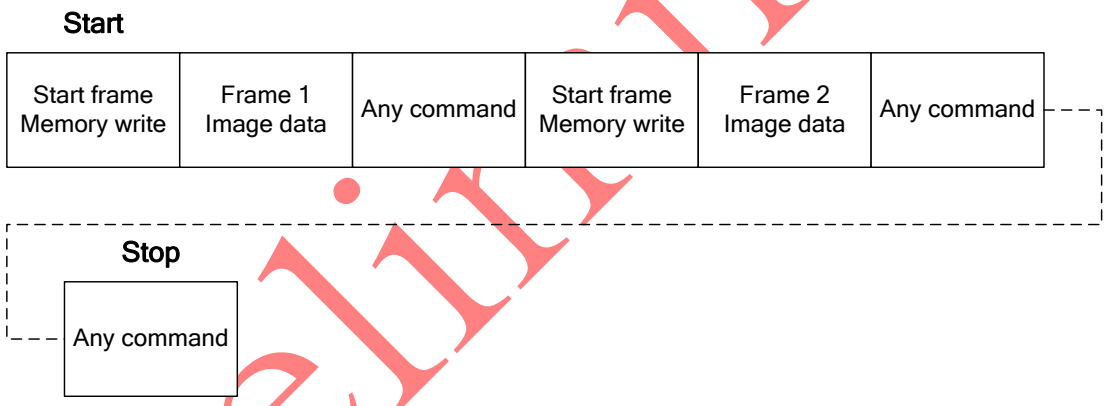
8.7.1 Method 1

The image data is sent to the frame memory in successive frame writes, each time the frame memory is filled, the frame memory pointer is reset to the start point and the next frame is written.



8.7.2 Method 2

The image data is sent and at the end of each frame memory download, a command is sent to stop frame memory write. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These apply to all data transfer Color modes on both serial and parallel interfaces.

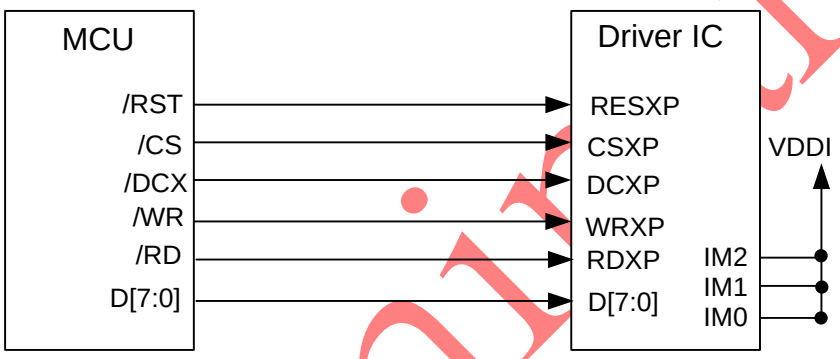
Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

8.8 Data Color Coding

8.8.1 8080 Series 8-bit Parallel Interface

The 8080 series 8-bit parallel interface of ST77922 can be used by setting IM[2:0]=”111b”. Different display data formats are available for two Colors depth supported by listed below.

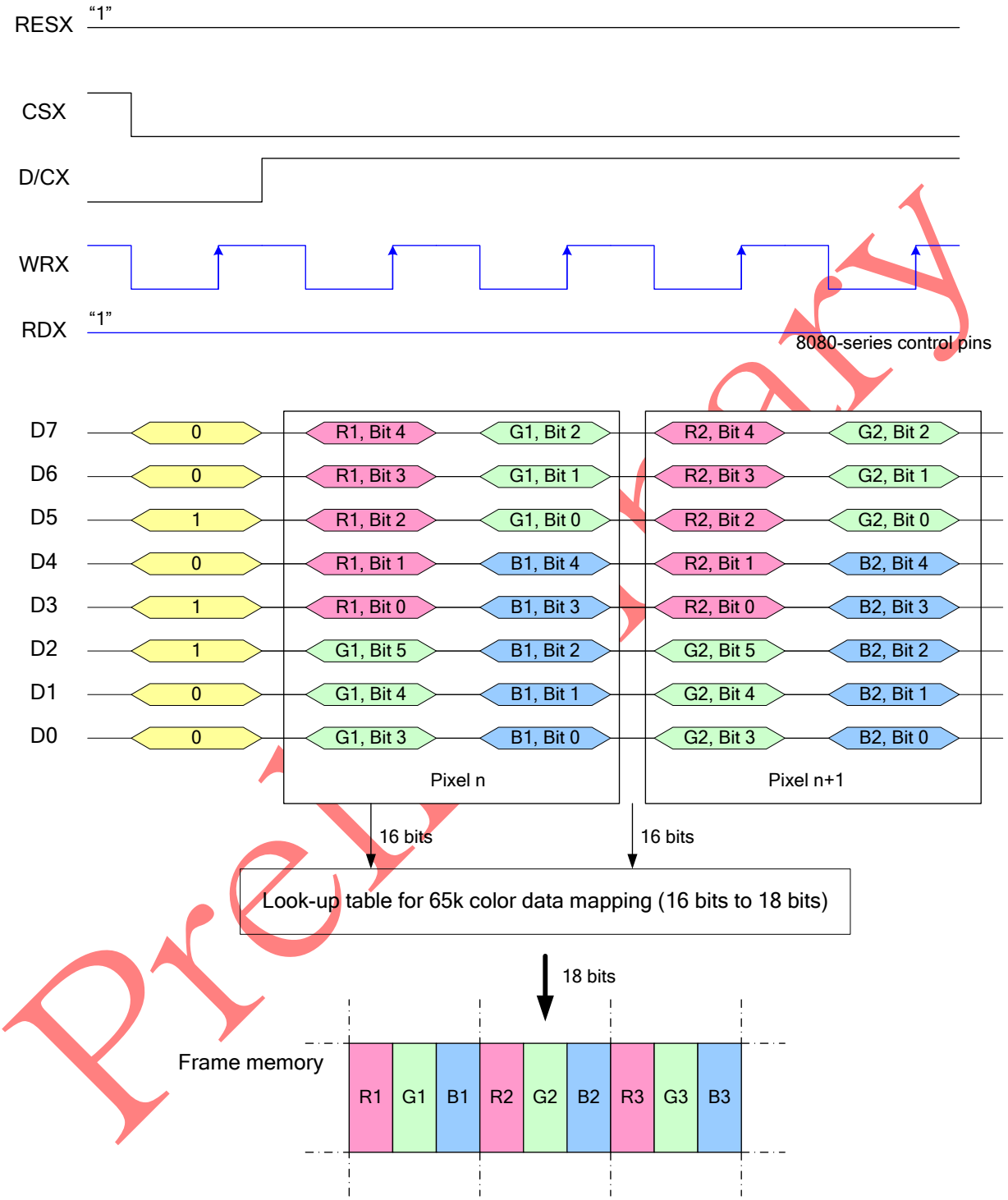
- 65k colors, RGB 5,6,5-bit input.
- 262k colors, RGB 6,6,6-bit input.
- 16.7M colors, RGB 8,8,8-bit input.



8080 Series 8-bit Interface Connection

8.8.1.1 8-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3Ah="01h"

There is 1pixel (3 sub-pixels) per 2-byte



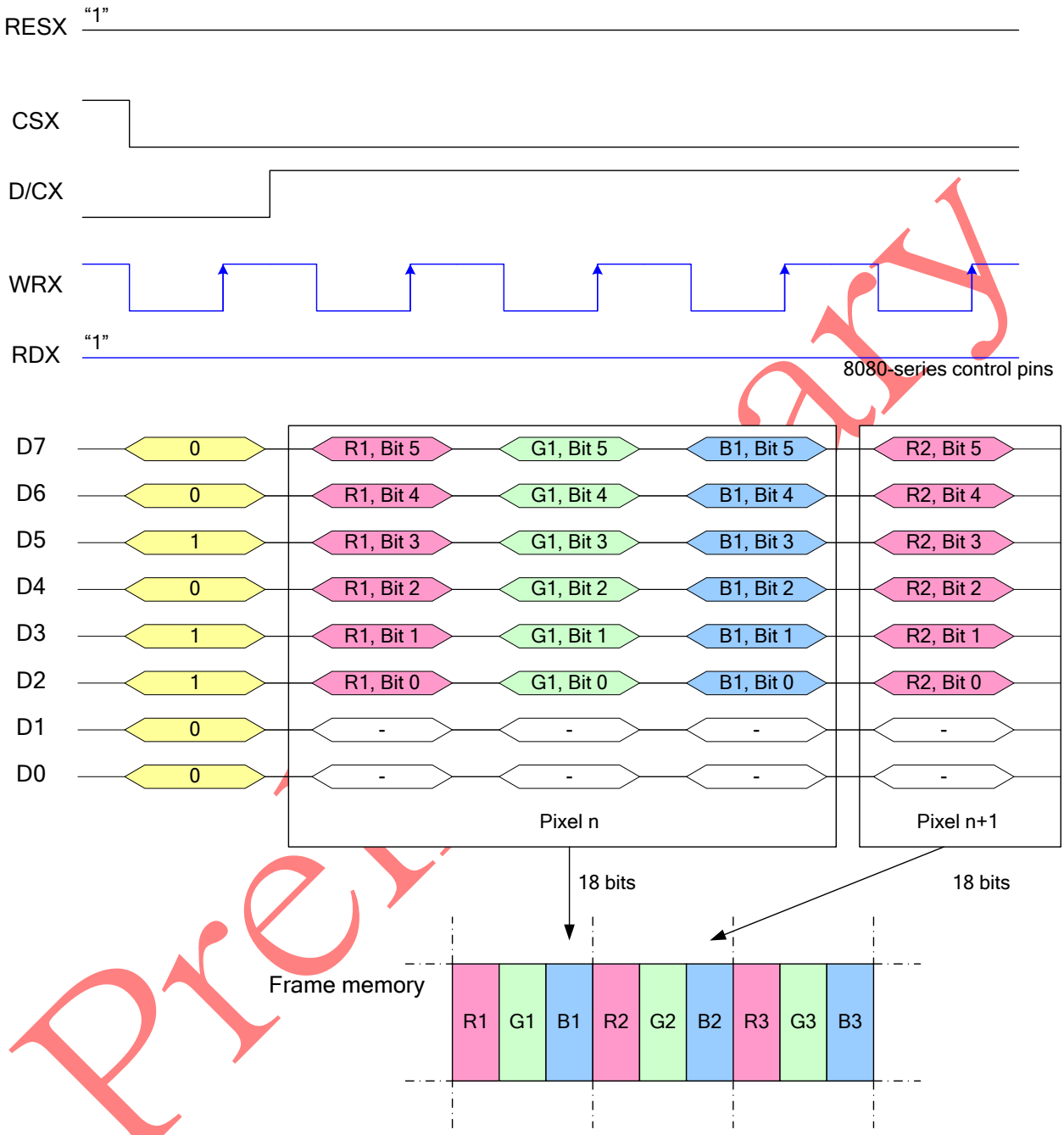
Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

8.8.1.2 8-bit data bus for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah="02h"

There is 1pixel (3 sub-pixels) per 3-bytes.



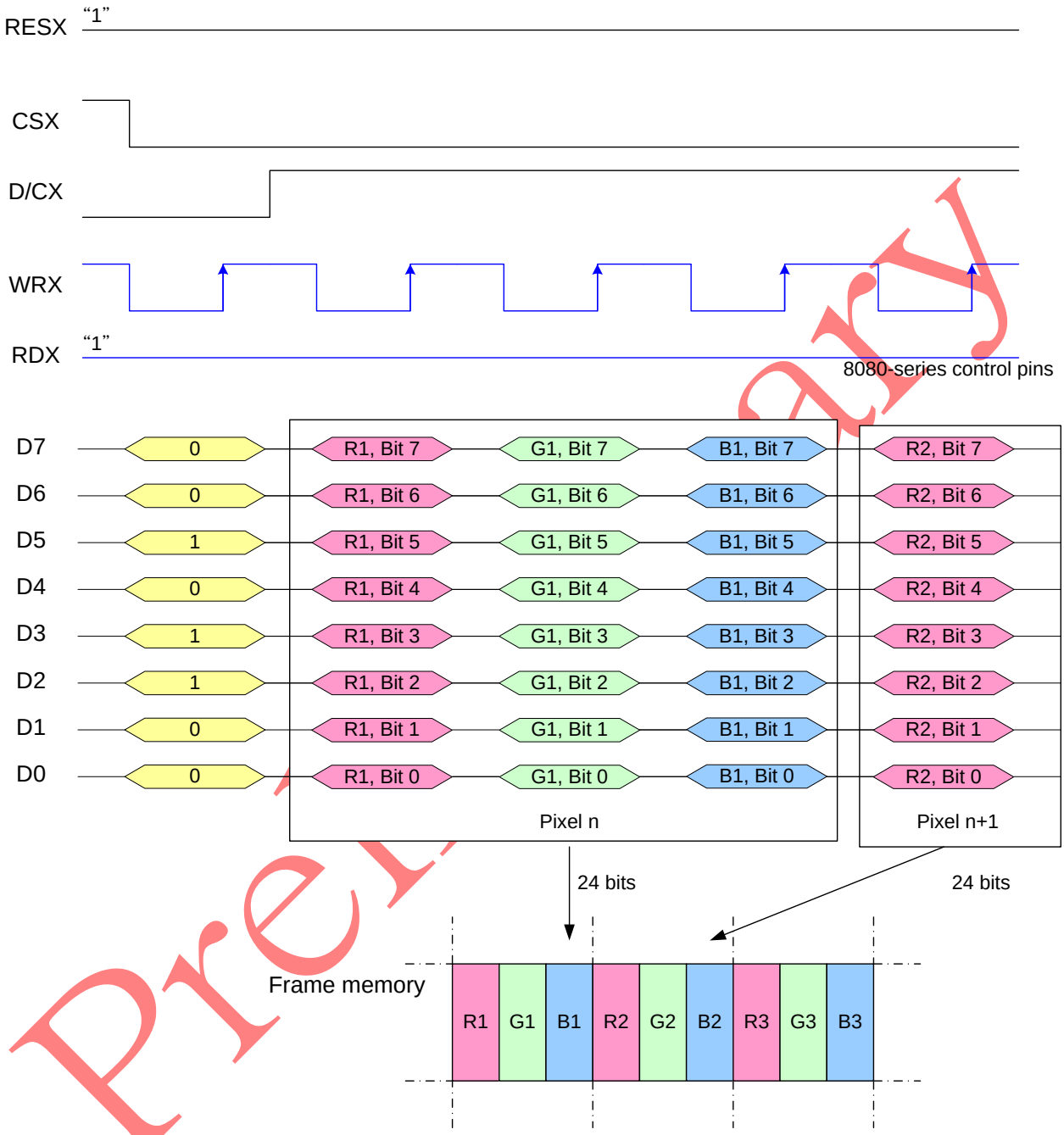
Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

8.8.1.3 8-bit data bus for 24-bit/pixel (RGB-8-8-8-bit input), 16.7M-Colors, 3Ah="03h"

There is 1pixel (3 sub-pixels) per 3-bytes.



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 7, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 24-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

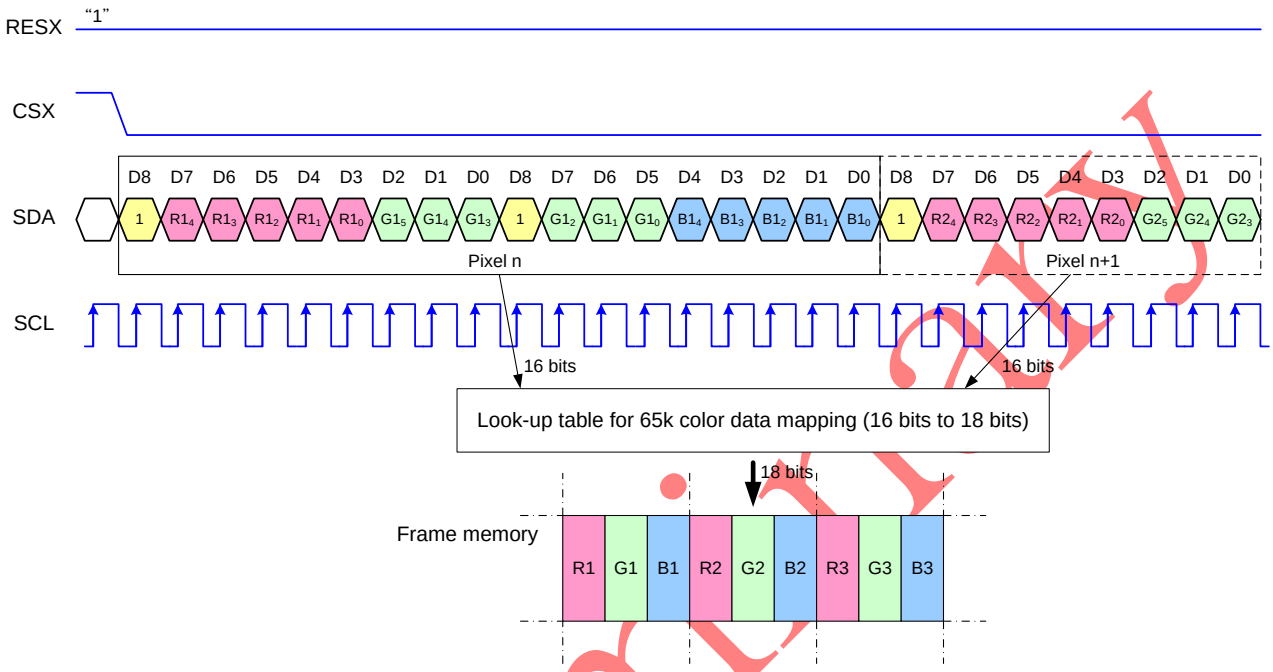
8.8.2 3-Line Serial Interface

Different display data formats are available for two colors depth supported by the LCM listed below.

65k colors, RGB 5-6-5-bit input

262k colors, RGB 6-6-6-bit input

8.8.2.1 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3Ah=”01h”

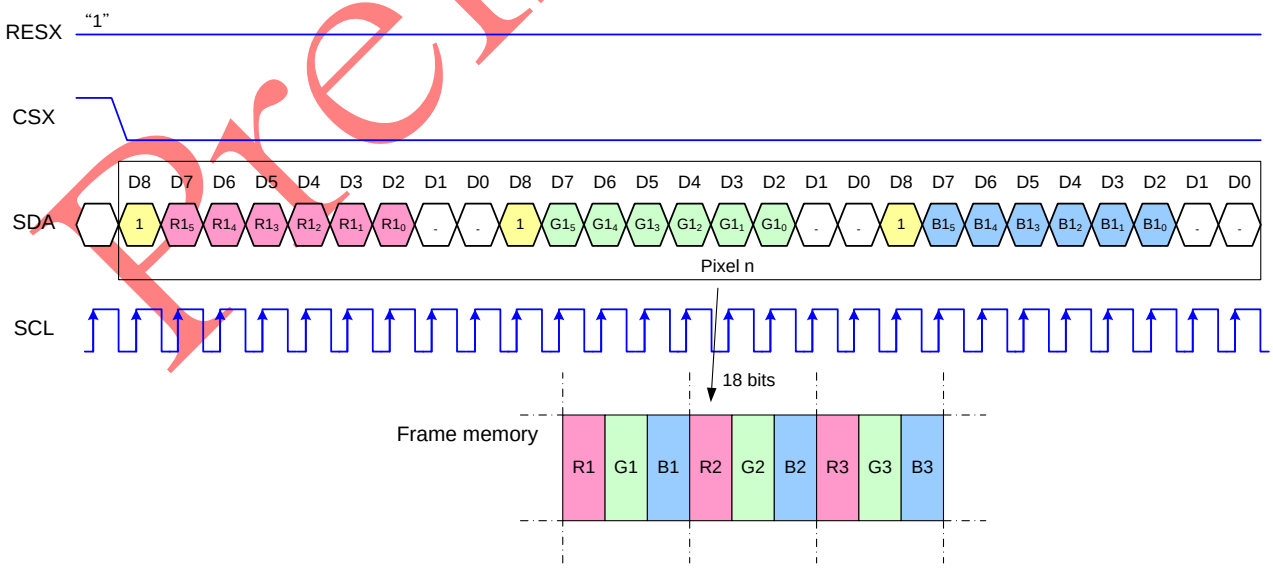


Note 1: Pixel data with the 16-bit color depth information

Note 2: The most significant bits are: Rx4, Gx5 and Bx4

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

8.8.2.2 Write data for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah=”02h”

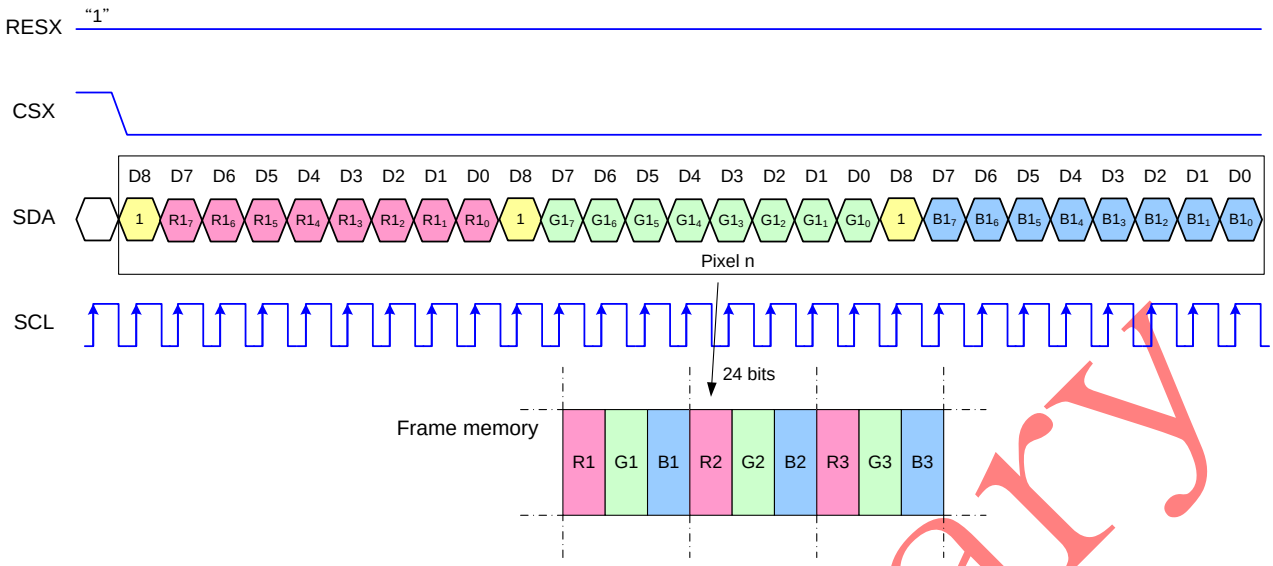


Note 1: Pixel data with the 18-bit color depth information

Note 2: The most significant bits are: Rx5, Gx5 and Bx5

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

8.8.2.3 Write data for 24-bit/pixel (RGB-8-8-8-bit input), 16.7M-Colors, 3Ah="03h"



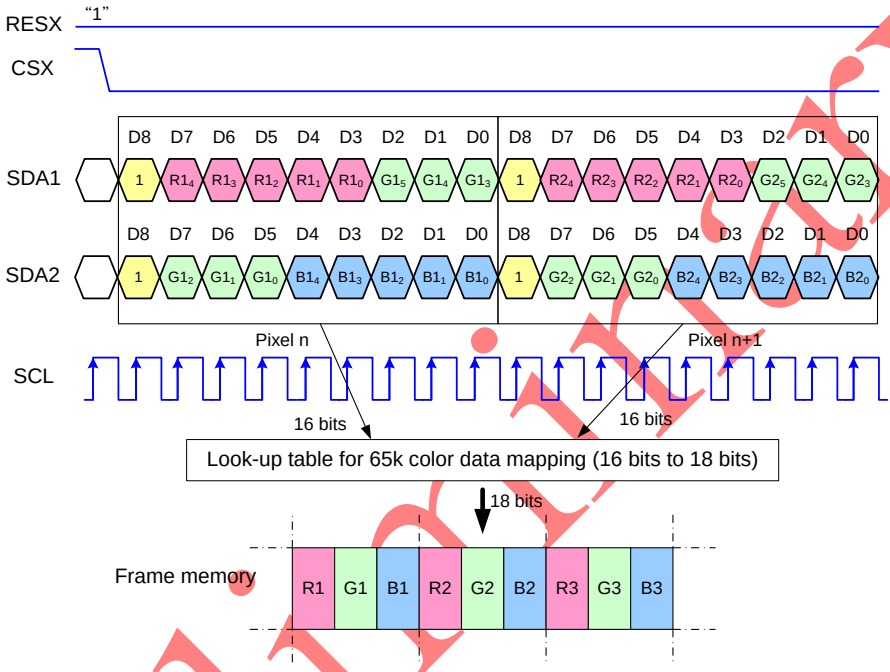
Note 1: Pixel data with the 24-bit color depth information
Note 2: The most significant bits are: Rx7, Gx7 and Bx7
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

8.8.3 2 Data Lane Serial Interface

Different display data formats are available for two colors depth supported by the LCM listed below.

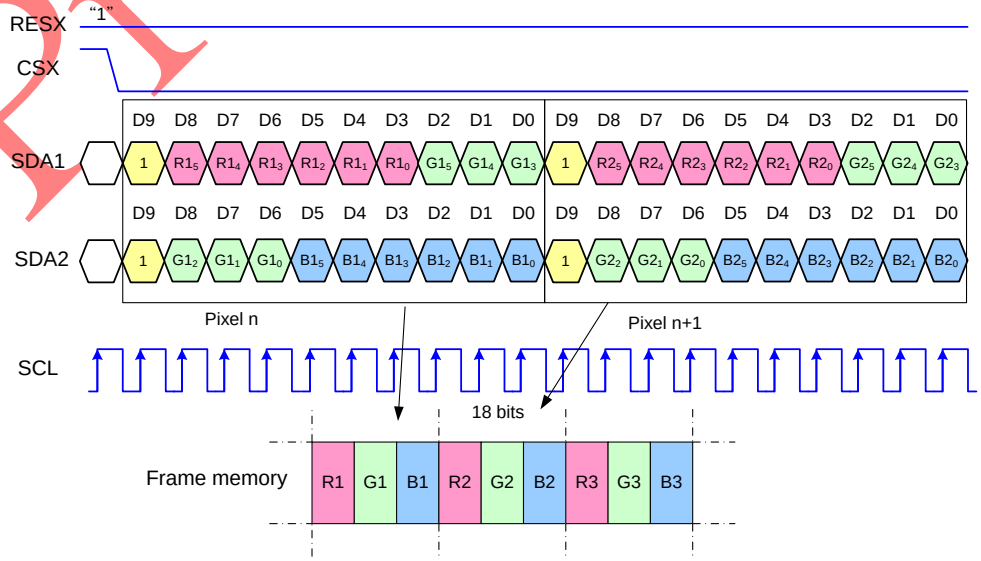
- 65k colors, RGB 5-6-5-bit input
- 262k colors, RGB 6-6-6-bit input
- 16.7M colors, RGB 8-8-8-bit input

8.8.3.1 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3Ah="01h"



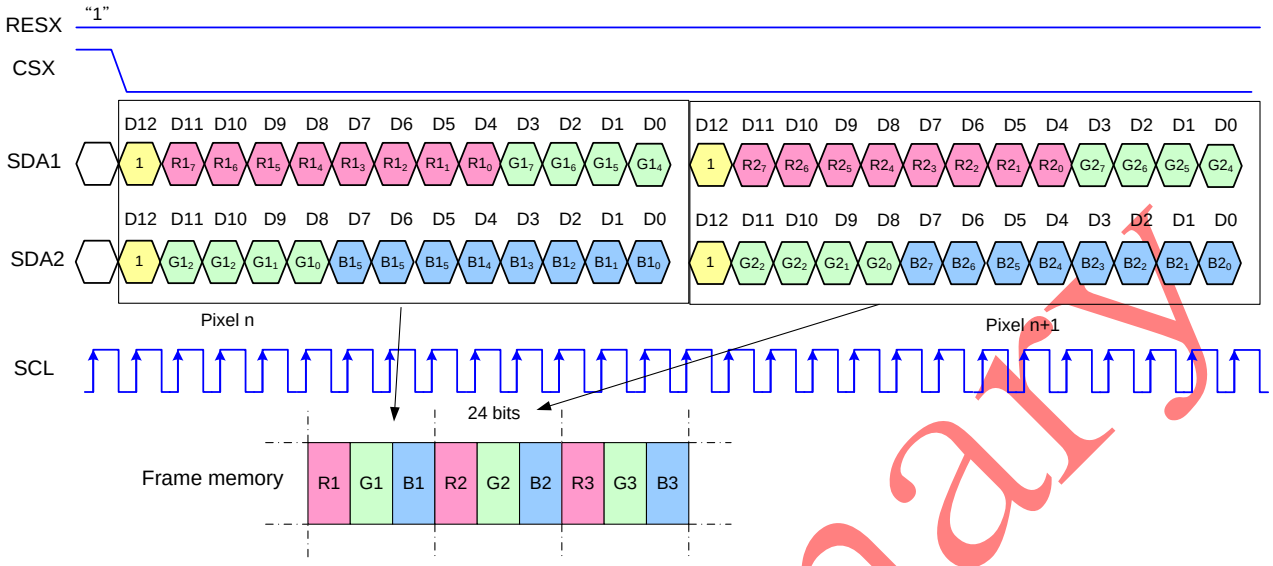
Note 1: Pixel data with the 16-bit color depth information
Note 2: The most significant bits are: Rx4, Gx5 and Bx4
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

8.8.3.2 Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3Ah="02h"



Note 1: Pixel data with the 18-bit color depth information
Note 2: The most significant bits are: Rx5, Gx5 and Bx5
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

8.8.3.3 Write data for 24-bit/pixel (RGB 8-8-8-bit input), 16.7M-Colors, 3Ah="03h"(TBD)



Note 1: Pixel data with the 24-bit color depth information
Note 2: The most significant bits are: Rx7, Gx7 and Bx7
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

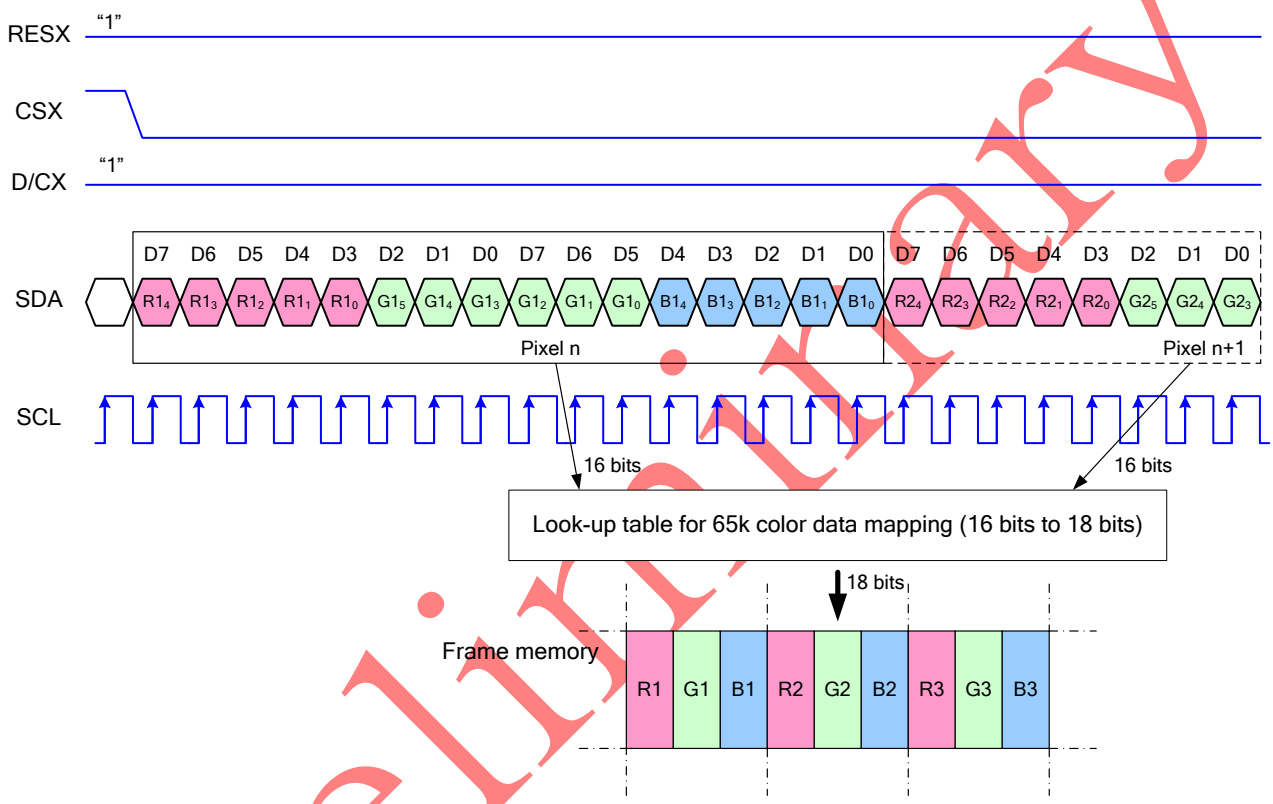
8.8.4 4-Line Serial Interface

Different display data formats are available for two colors depth supported by the LCM listed below.

65k colors, RGB 5-6-5-bit input

262k colors, RGB 6-6-6-bit input

8.8.4.1 Write data for 16-bit/pixel (RGB-5-6-5-bit input), 65K-Colors, 3Ah="01h"

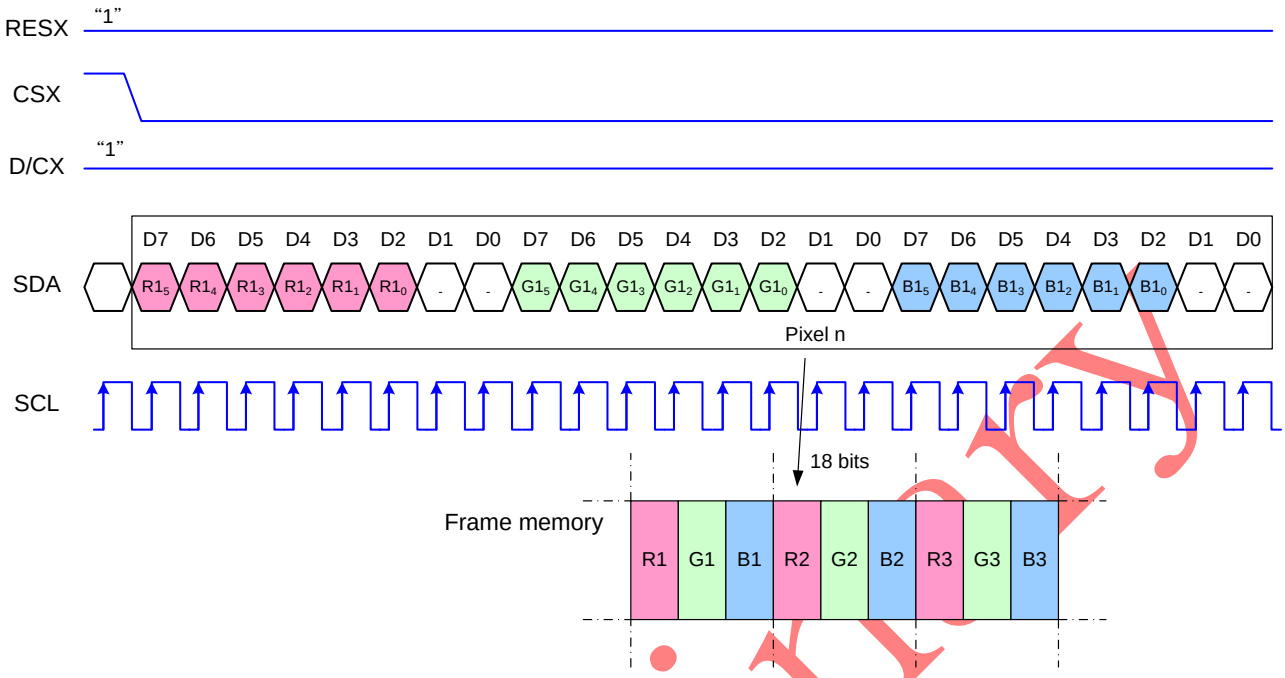


Note 1. Pixel data with the 16-bit color depth information

Note 2. The most significant bits are: Rx4, Gx5 and Bx4

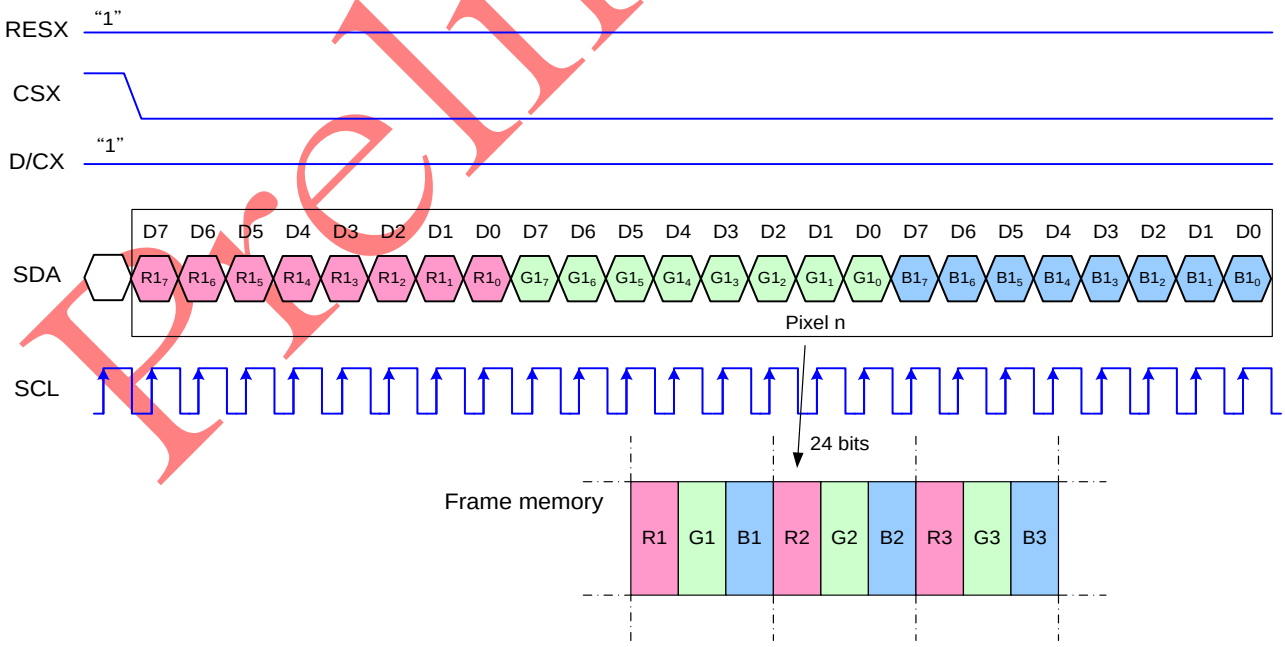
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

8.8.4.2 Write data for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah="02h"



Note 1. Pixel data with the 18-bit color depth information
Note 2. The most significant bits are: Rx5, Gx5 and Bx5
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

8.8.4.3 Write data for 24-bit/pixel (RGB-8-8-8-bit input), 16.7M-Colors, 3Ah="03h"



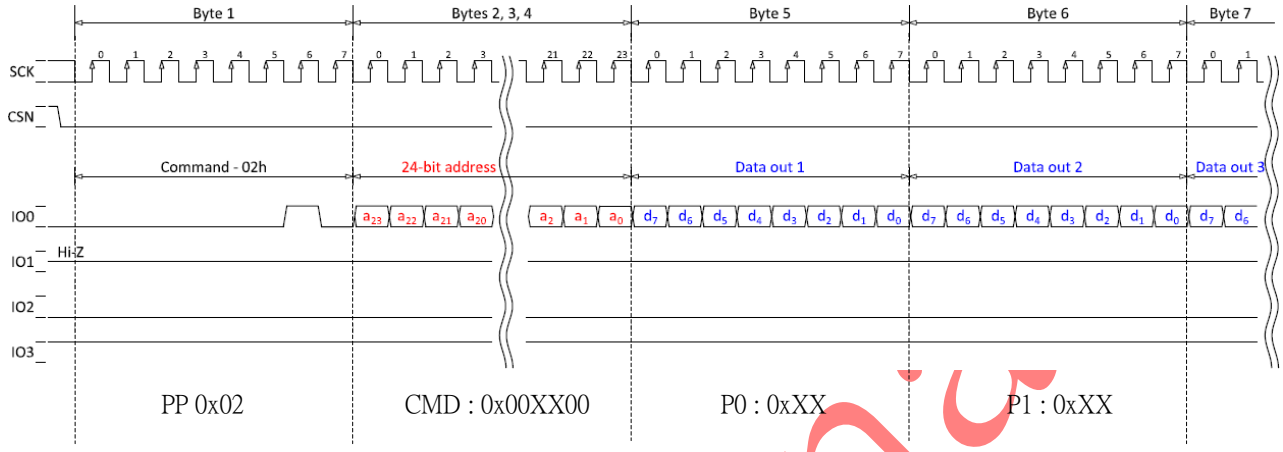
Note 1. Pixel data with the 24-bit color depth information
Note 2. The most significant bits are: Rx7, Gx7 and Bx7
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

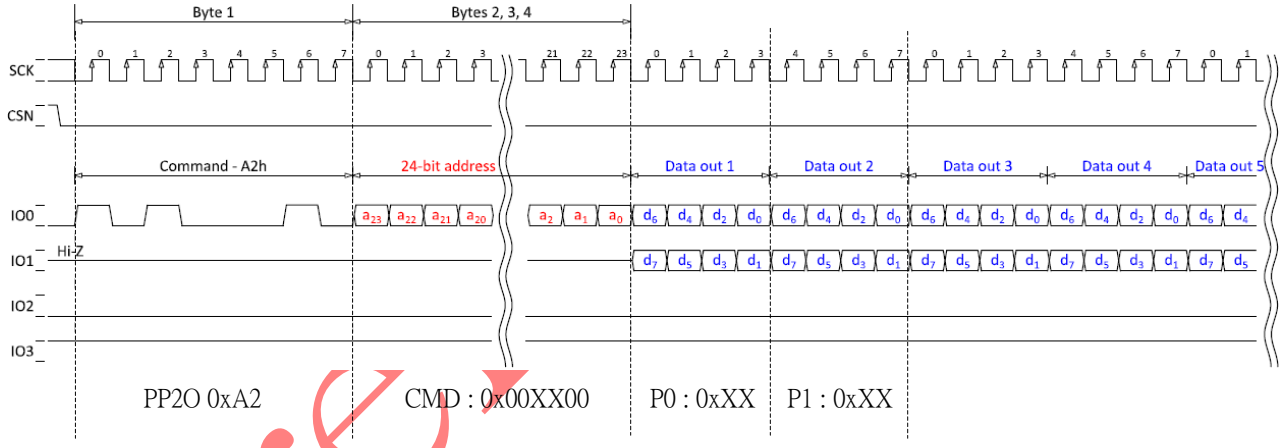
8.8.5 Quad-SPI Interface

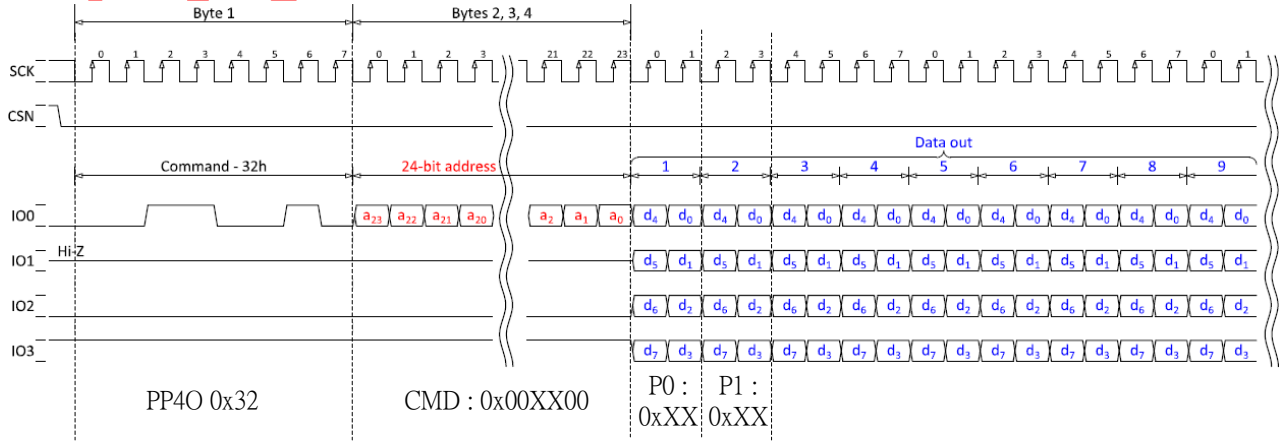
Pin Name	Description
CSX	Chip selection signal
RDX (SCL)	Clock signal
SDA	Serial input/output data lane 0
DCX	Serial input data lane 1
D0	Serial input data lane 2
D1	Serial input data lane 3

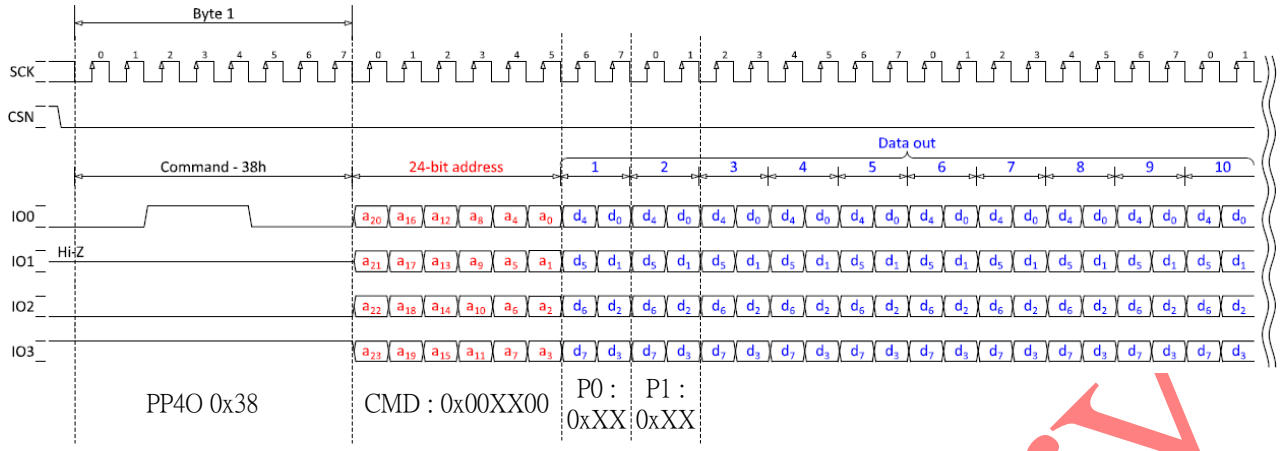
8.8.5.1 Command write mode:

When host writes commands or parameter to ST77922, host needs to send 1 byte of write command instruction (0x02、0xA2、0x32 or 0x38). Then host sends 3 bytes of AD[23:0] which is composed of 1 byte of 0x00, 1 byte of command address and 1 byte of 0x00. After host sending instruction and AD[23:0], the following data is parameter (are parameters). When the last bit of parameter has been sent, CSX pin should be returned “H” level.



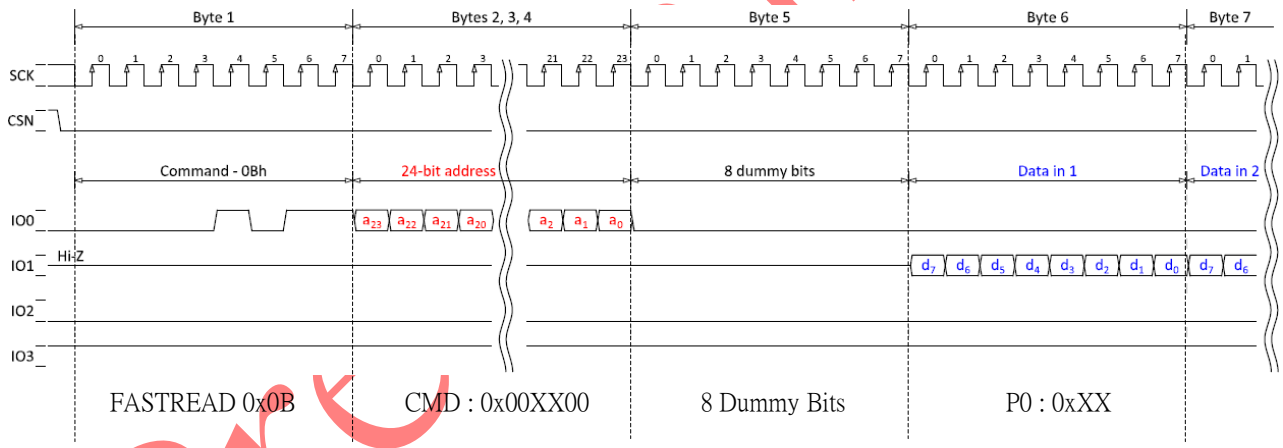






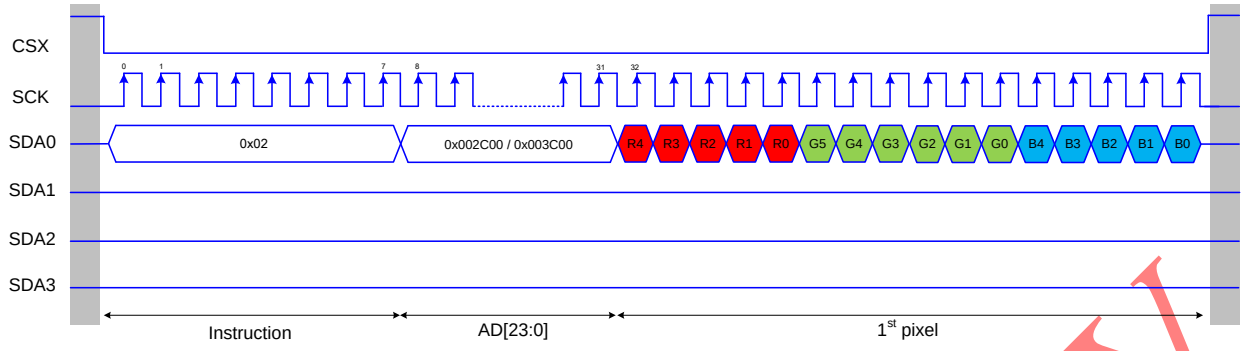
8.8.5.2 Read command mode

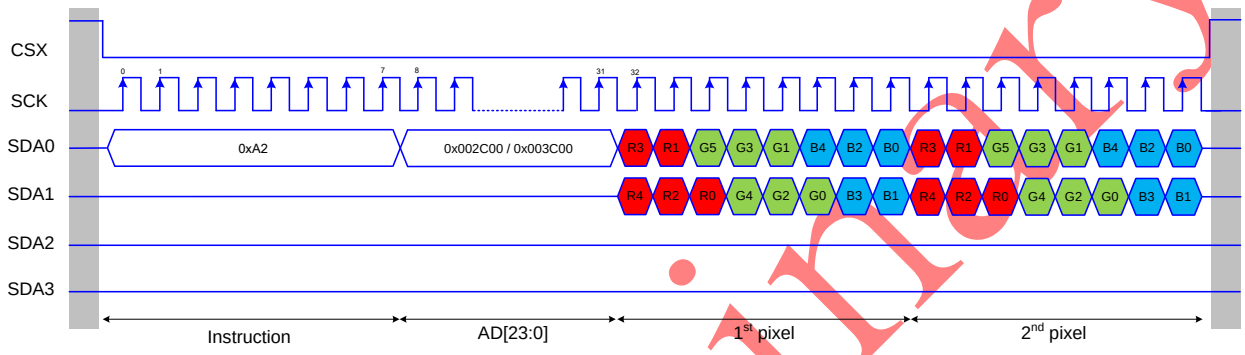
When host reads commands or parameter to ST77922, host needs to send 1 byte of write command instruction (0x0B). Then host sends 3 bytes of AD[23:0] which is composed of 1 byte of 0x00, 1 byte of command address and 1 byte of 0x00. After host sending read command and AD[23:0], the following output data is command address parameter (are parameters). When the last bit of parameter has been output, CSX pin should be returned “H” level.

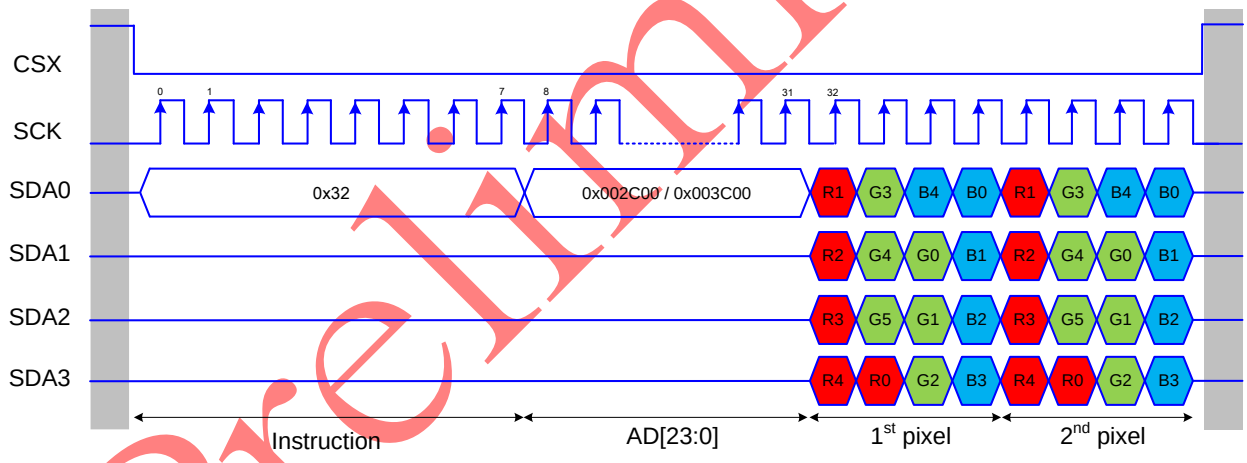


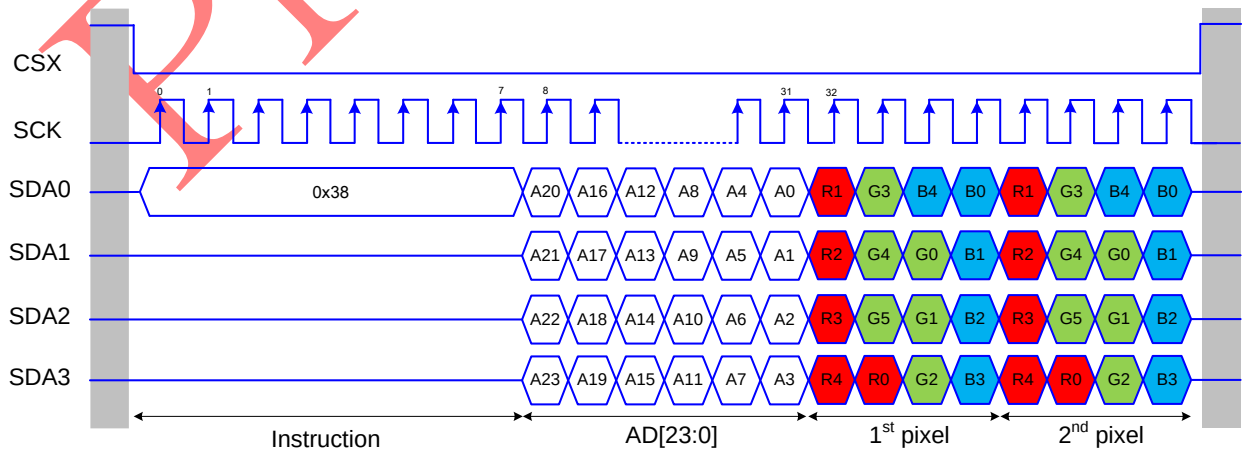
8.8.5.3 Color Format

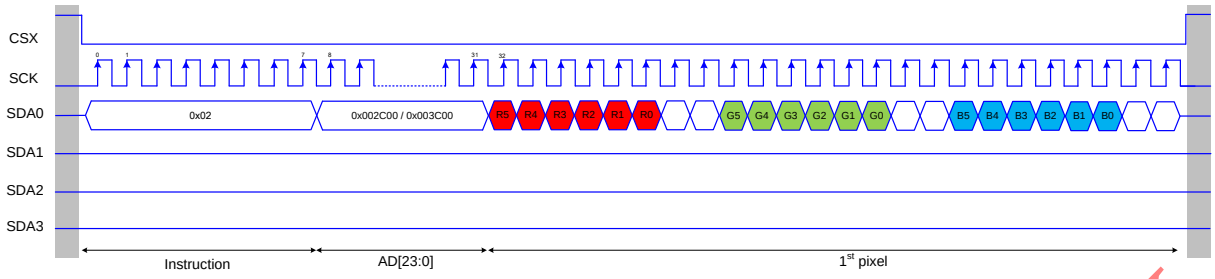
QSPI RGB565

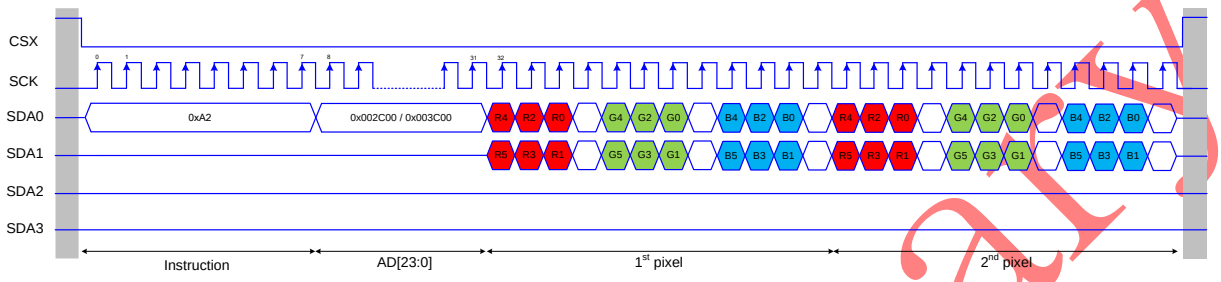


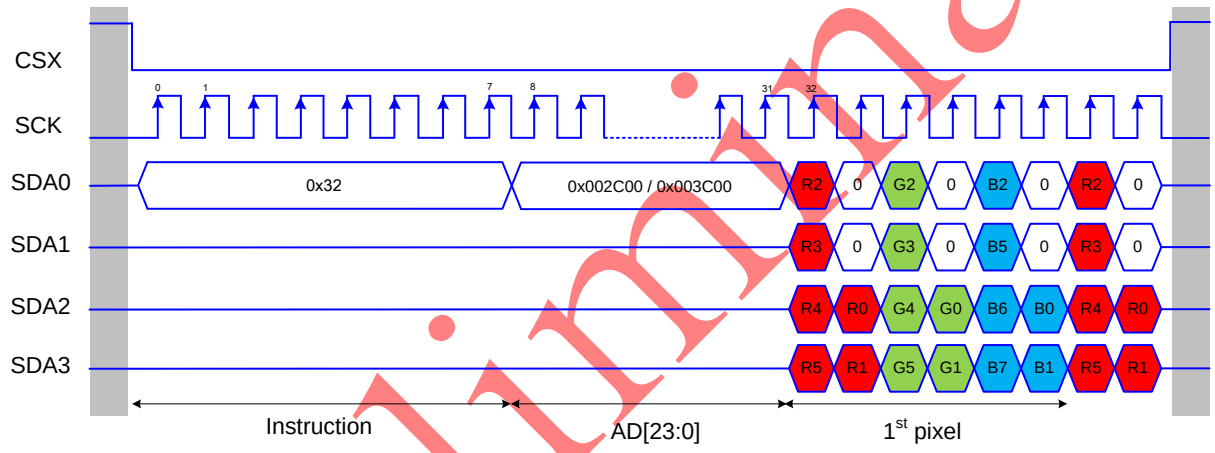


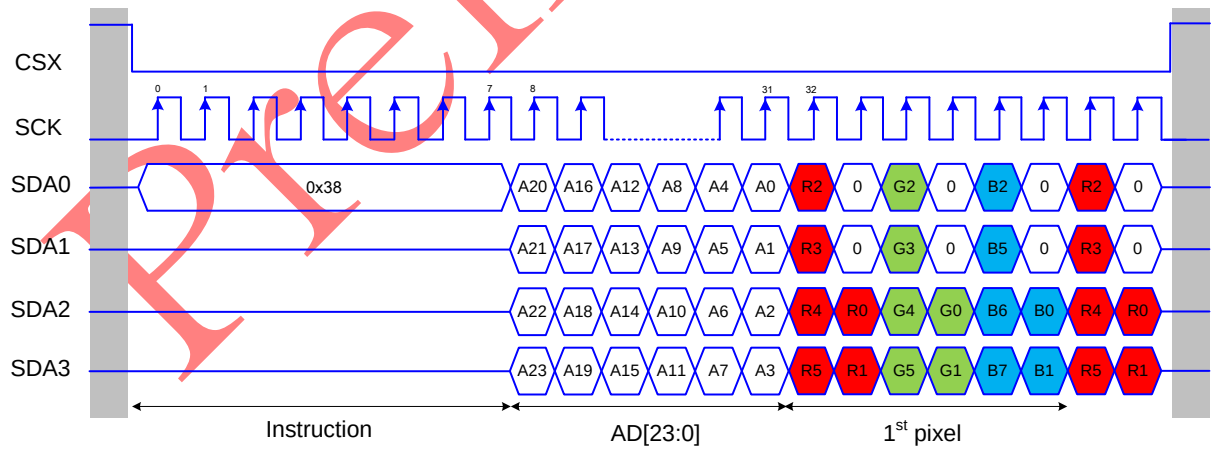




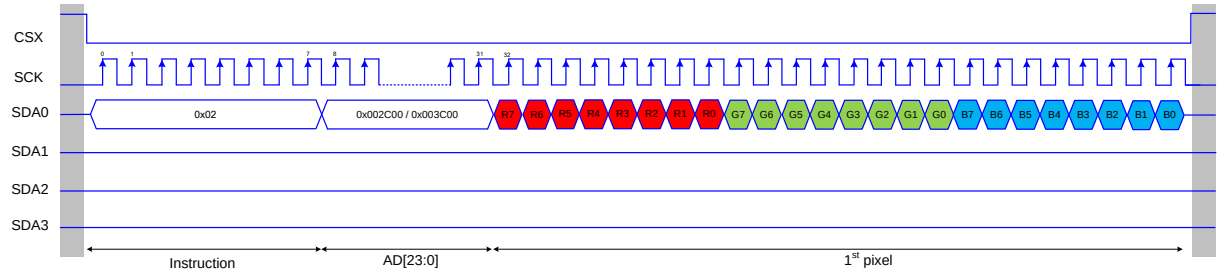


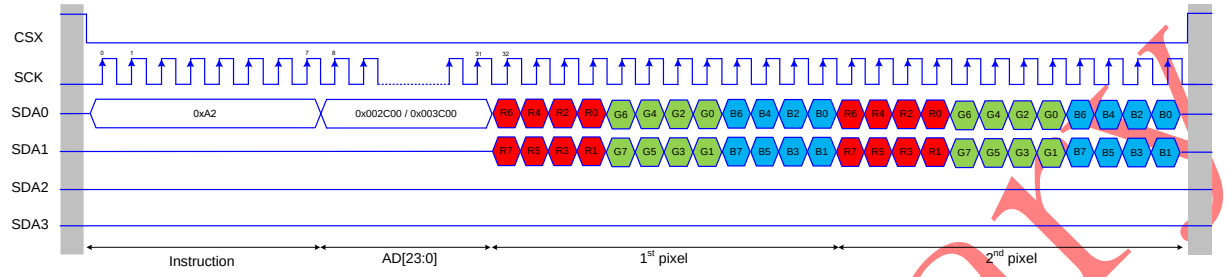


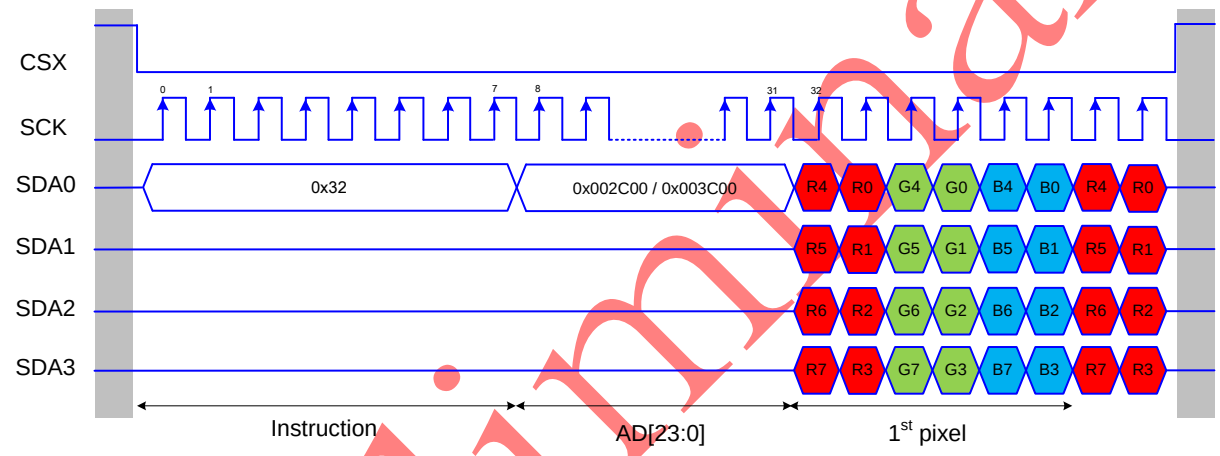


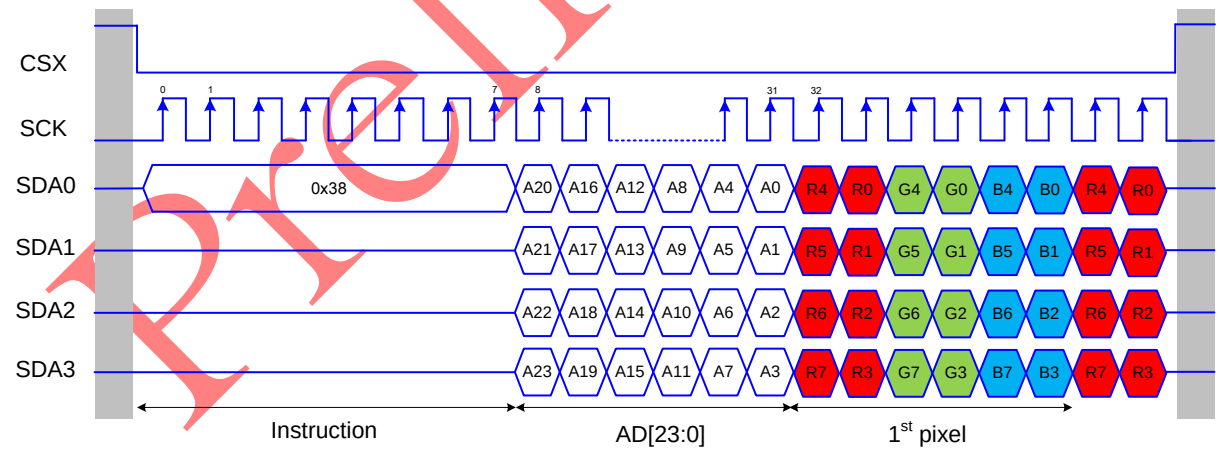


QSPI RGB888









8.9 RGB Interface

8.9.1 RGB interface Selection

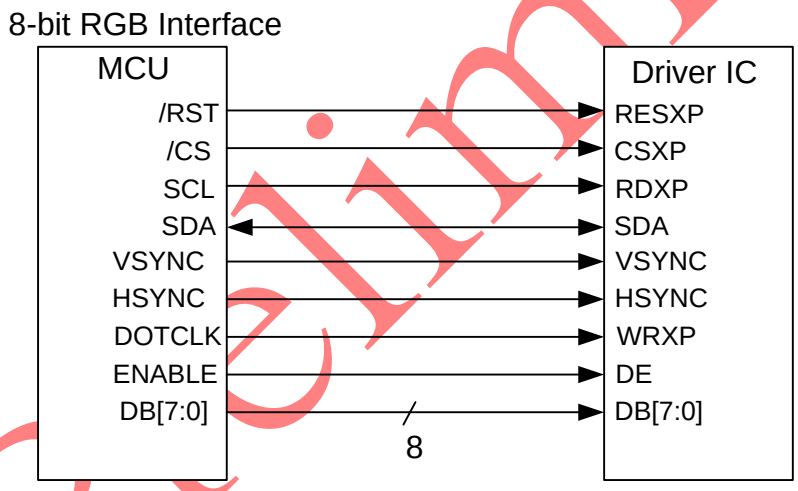
The color format selection of RGB Interface for ST77922 is selected by setting the command 3Ah, DB [1:0].

RGB Interface Mode	3Ah, DB[1:0]	Data pins
8-bit 16.7M RGB Interface	11	DB[7:0]
8-bit 262K RGB Interface	10	DB[7:0]
8-bit 65K RGB Interface	01	DB[7:0]

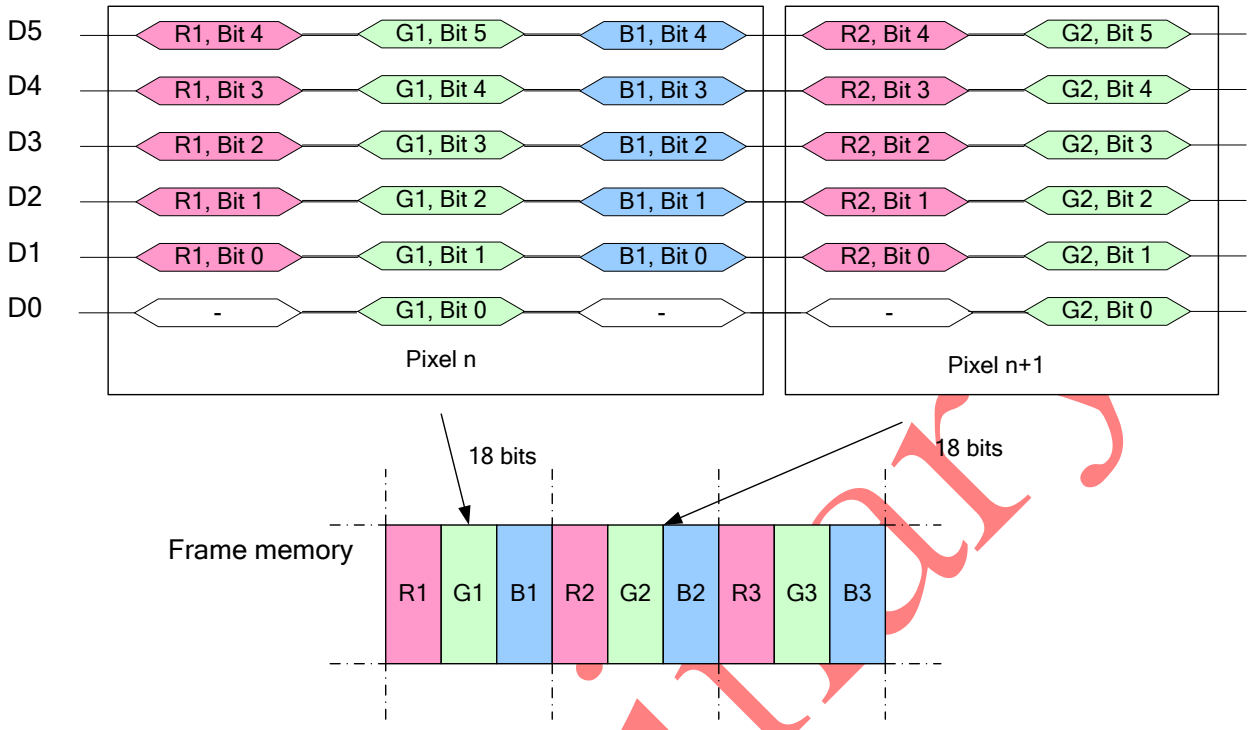
8.9.2 RGB Color Format

ST77922 supports two kinds of RGB interface, DE mode and HV mode, and 6bit data format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, DE, DB[7:0] pins can be used; when HV mode is selected and the VSYNC, HSYNC, DOTCLK, D[5:0] pins can be used. When using RGB interface, only serial interface can be selected.

8-bit RGB interface & 3-line serial interface hardware suggestion, IM[2:0]=100.
8-bit RGB interface & 4-line serial interface hardware suggestion, IM[2:0]=101.



Write data for 6-bit/pixel (RGB 5-6-5-bit input), 65K-Colors



Write data for 6-bit/pixel (RGB 6-6-6-bit input), 262K-Colors

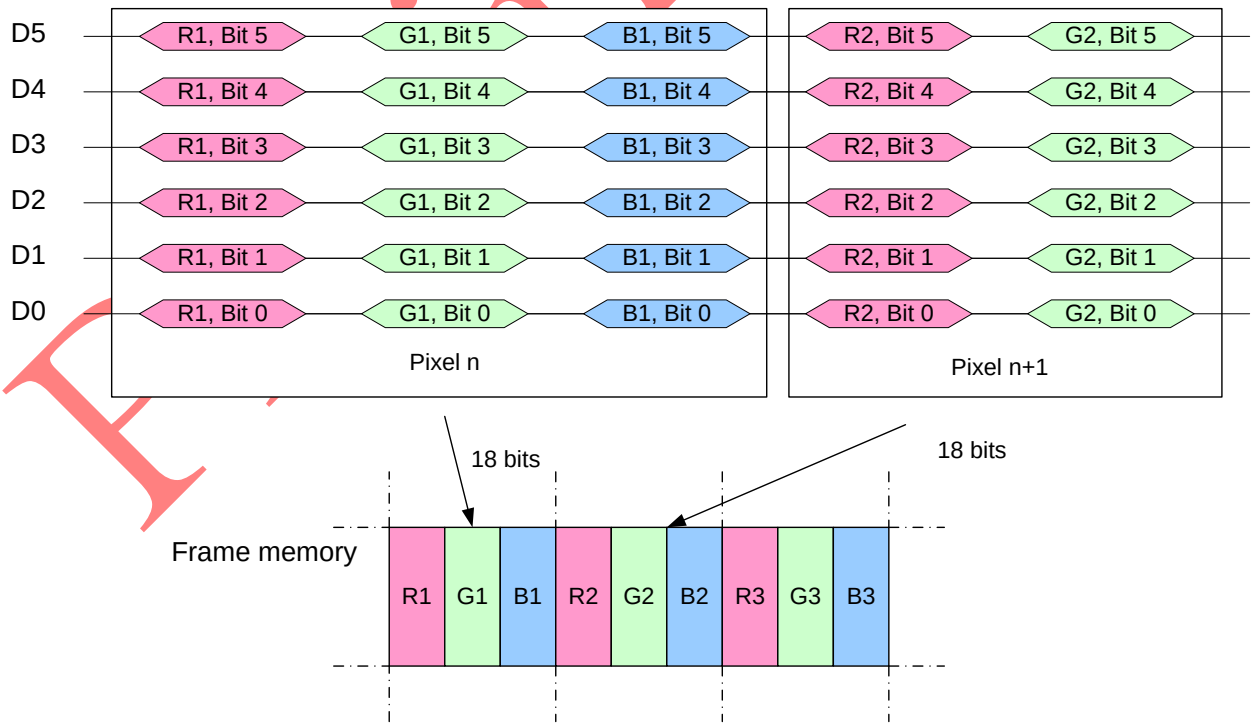


Figure 23 RGB Interface Data Format

8.9.3 RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.

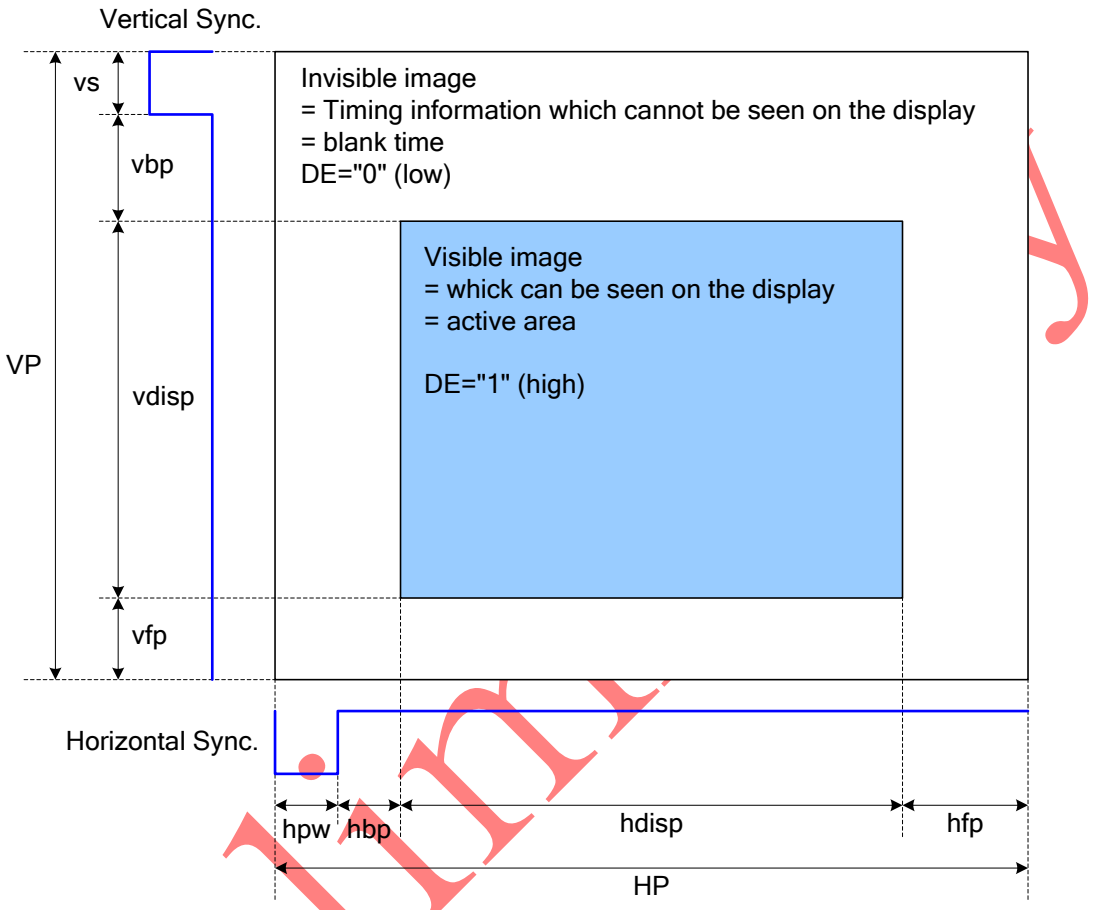


Figure 24 DRAM Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

8bit RGB interface:

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	2	-	-	Clock
Horizontal Sync. Back Porch	hbp	2	-	-	Clock
Horizontal Sync. Front Porch	hfp	2	-	-	Clock
Vertical Sync. Width	vs	2	-	-	Line
Vertical Sync. Back Porch	vbp	2	-	127	Line
Vertical Sync. Front Porch	vfp	2	-	1023	Line

Note:

1.Typical value are related to the setting of frame rate is 60Hz.

2.Touch Controller operation time was considered

3.The minimum values of this table mean the limitation of IC without considering the panel GIP

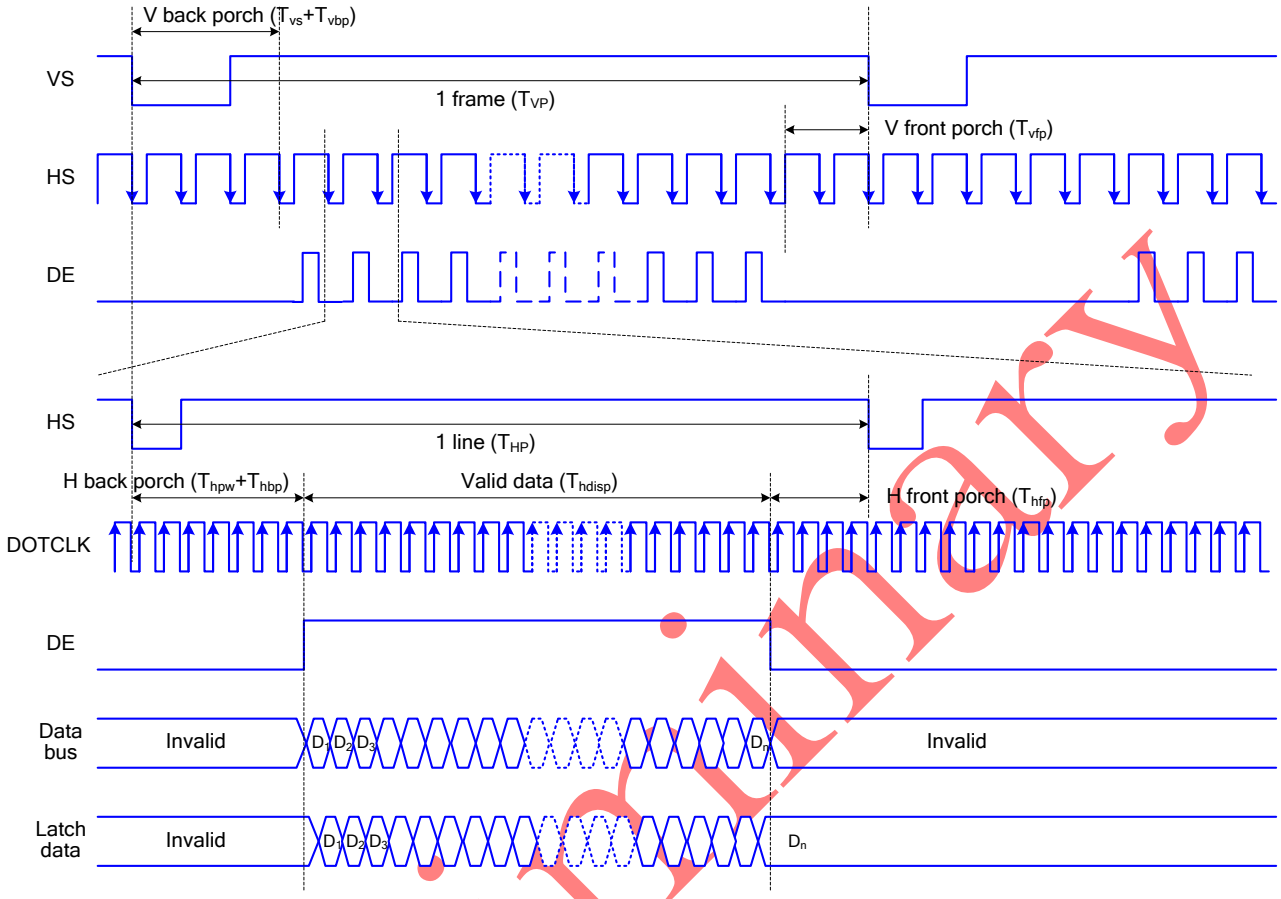
8.9.4 RGB Interface Mode Selection

ST77922 supports two kinds of RGB interface, DE mode and HV mode. Each mode also can select with ram and without ram. The table shown below uses command BDh, DB[7] to select with ram and without ram.

RCM	RGB Mode	WO	Data Path
0	DE mode	0	Ram
		1	Shift register (without Ram)
1	HV mode	0	Ram
		1	Shift register (without Ram)

8.9.5 RGB Interface Timing

The timing chart of RGB interface DE mode is shown as follows.



Note: The setting of front porch and back porch in host must match that in IC as this mode.

Figure 25 Timing Chart of Signals in RGB Interface DE Mode

The timing chart of RGB interface HV mode is shown as follows.

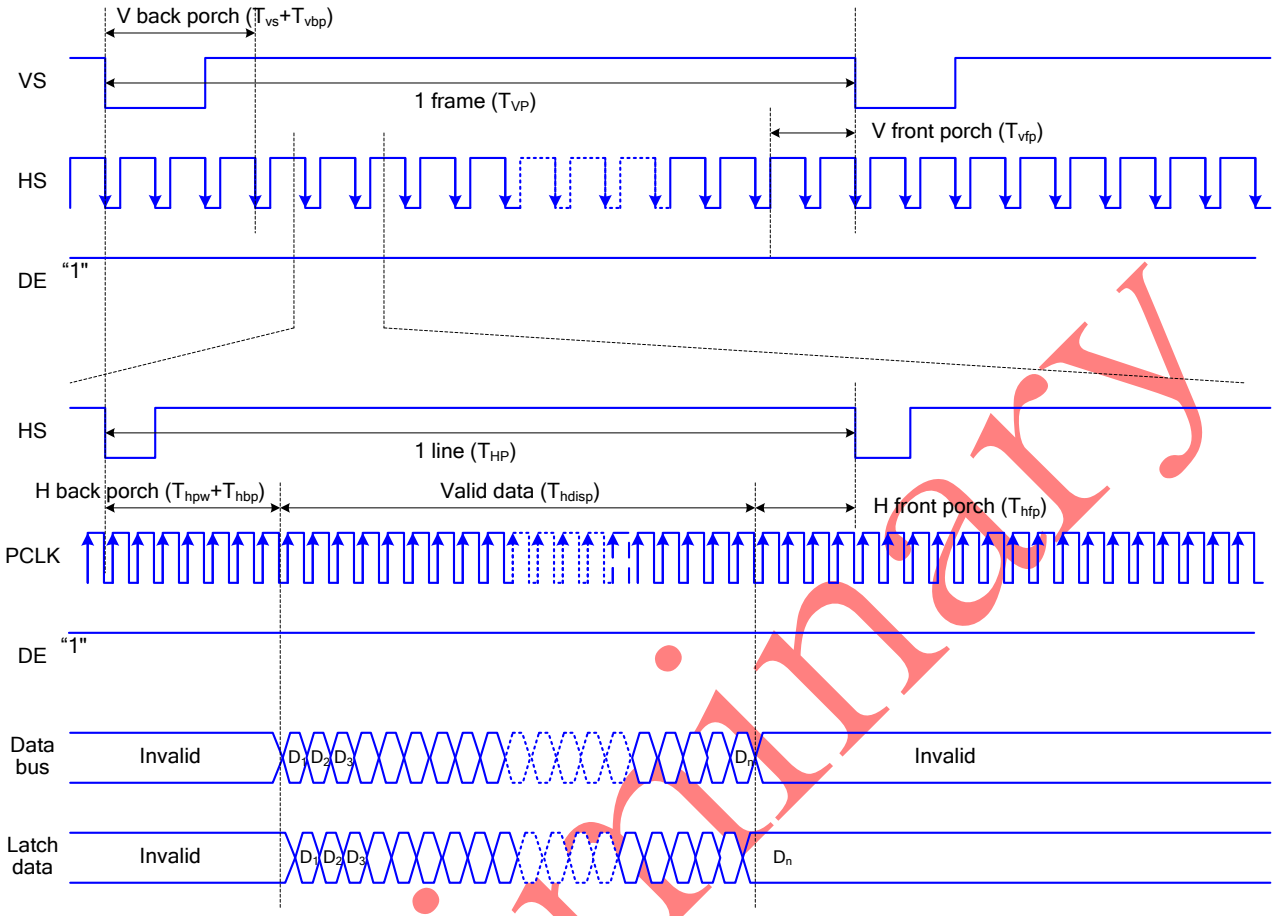


Figure 26 Timing chart of RGB interface HV mod

The following are the functions not available in RGB Input Interface mode.

Function	RGB Interface	I80 System Interface
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

VSYNC, HSYNC, and DOTCLK signals must be supplied during a display operation period.

In RGB interface mode, the panel controlling signals are generated from DOTCLK, not the internal clock generated from the internal oscillator.

In 8-bit RGB interface mode, each of RGB dots are transferred in synchronization with DOTCLK signals. In other words, one pixel data needs to take three DOTCLKs to transfer.

In 8-bit RGB interface mode, the cycles of VSYNC, HSYNC, ENABLE, DOTCLK signals must be set correctly so that the data transfer is completed in units of pixels.

When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.

In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.

In RGB interface mode, a RAM address is set in the address counter every frame on the falling edge of VSYNC.

8.10 Mobile Industry Processor Interface (MIPI)

8.10.1 Display Serial Interface (DSI)

8.10.1.1 GENAL DESCRIPTION

The communication can be separated 2 different levels between the MCU and the display module:

1. Low level communication what is done on the interface level
2. High level communication what is done on the packet level

8.10.1.2 Interface Level Communication

The display module uses data and clock lane differential pairs for DSI (DSI-1M). Both differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode. High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode. There are used different modes and protocols in each mode when there wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State	Line DC Voltage Levels		High Speed (HS)	Low Power	
	DATA_P	DATA_N	Burst Mode	CLOCK_P	CLOCK_N
HS-0	Low (HS)	High (HS)	Differential – 0	Note 1	Note1
HS-1	High (HS)	Low (HS)	Differential – 1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS – Request	Mark – 0
LP-10	High (LP)	Low (LP)	Not Defined	LP – Request	Mark – 1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Notes:

(1) Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.

(2 If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

8.10.1.3 DSI-CLOCK Lanes

DSI-CLOCK_P/N lanes can be driven into three different power modes:

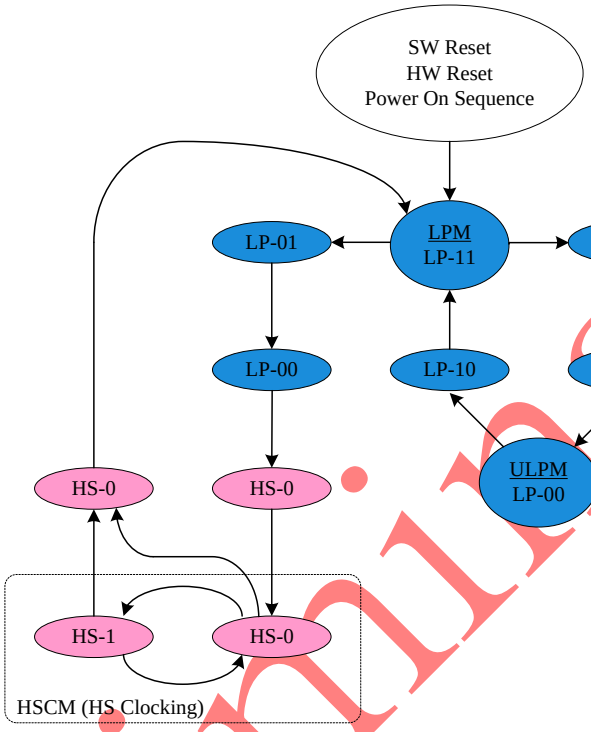
- Low Power Mode (LPM)
- Ultra Low Power Mode (ULPM)
- High Speed Clock Mode (HSCM)

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power

Mode (LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM). These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

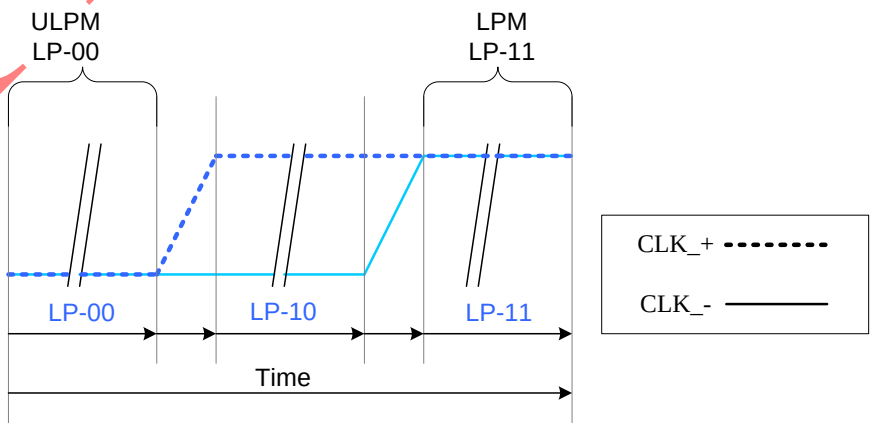


Flow chart of the different clock lanes

1. Low Power Mode (LPM)

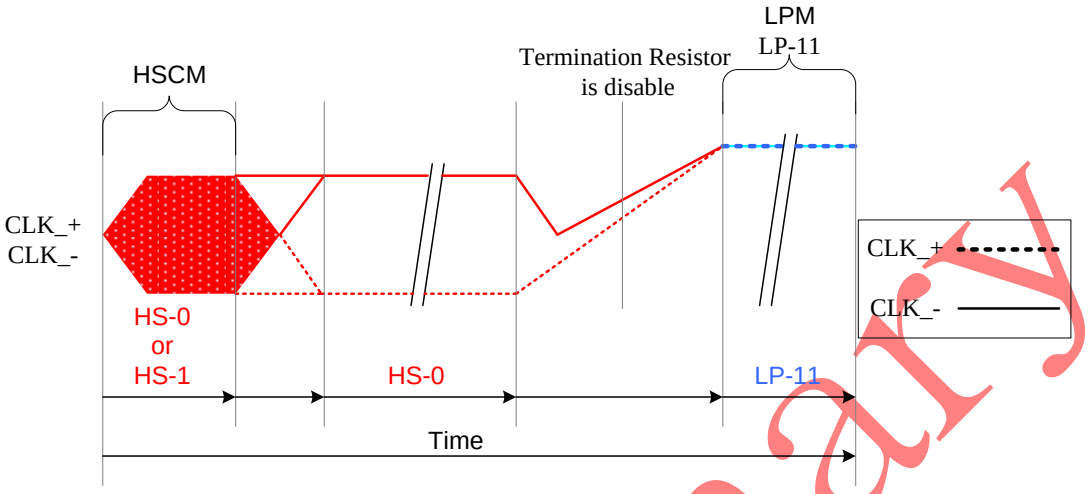
DSI-CLOCK_P/N lanes can be driven to the Low Power Mode (LPM), when DSI-CLOCK lanes are entering LP-11 State Code, in three different ways:

- After SW Reset, HW Reset or Power On Sequence =>LP-11 After DSI-CLOCK_P/N lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10
- LP-11 (LPM). This sequence is illustrated below.



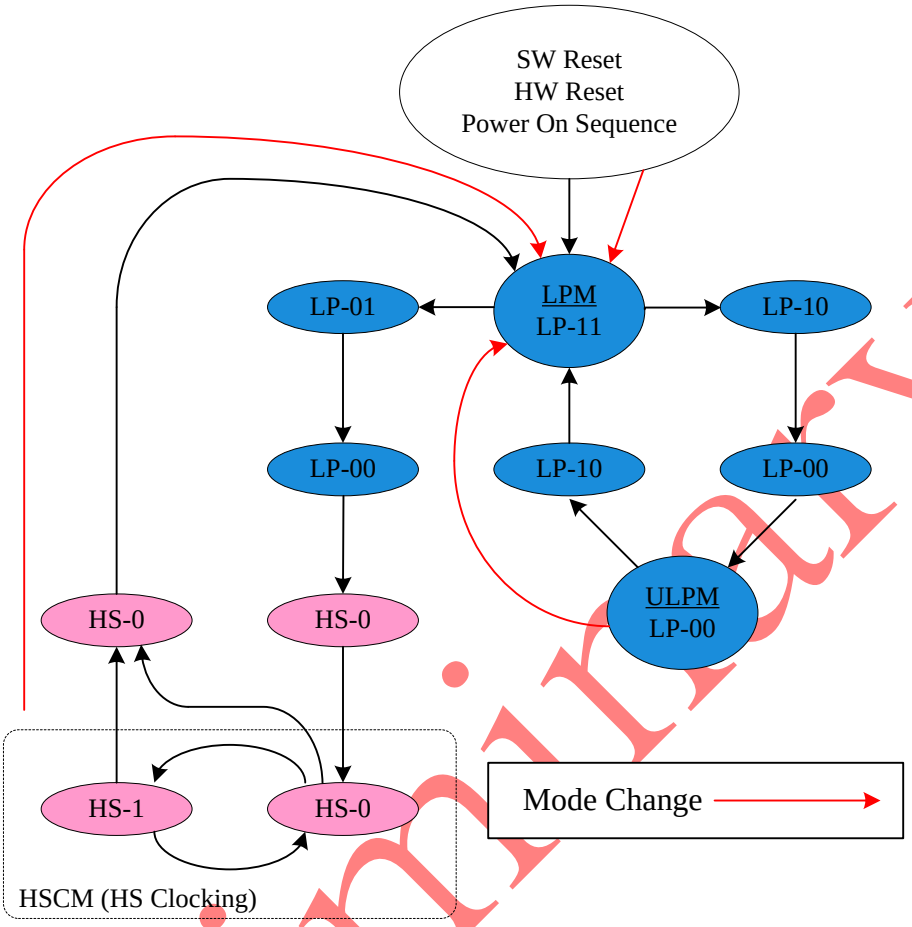
From ULPM to LPM

- After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0=>LP-11 (LPM). This sequence is illustrated below.



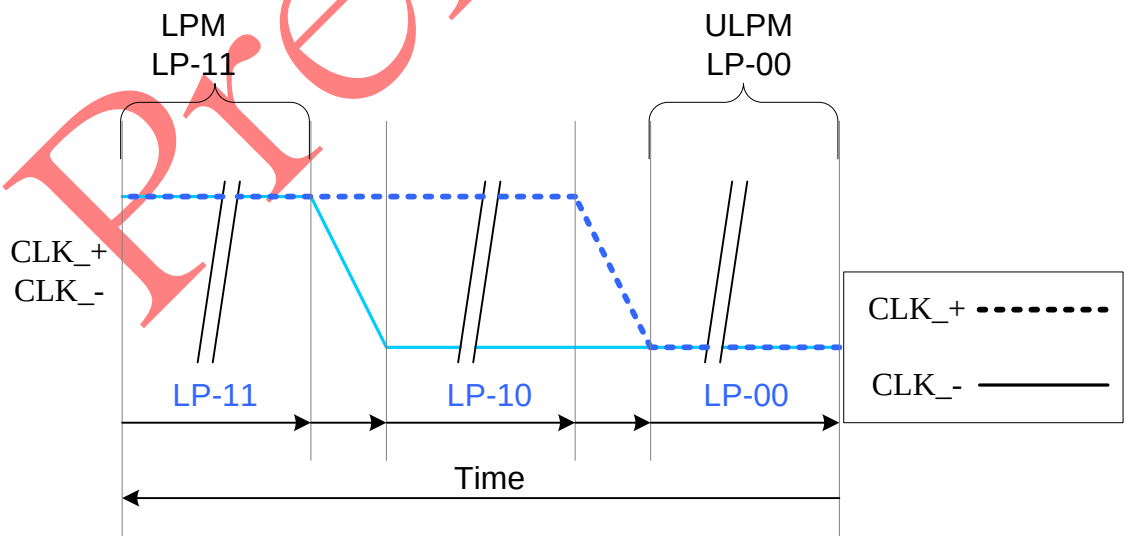
From High Speed Clock Mode (HSCM) to LPM

All three mode changes are illustrated a flow chart below.



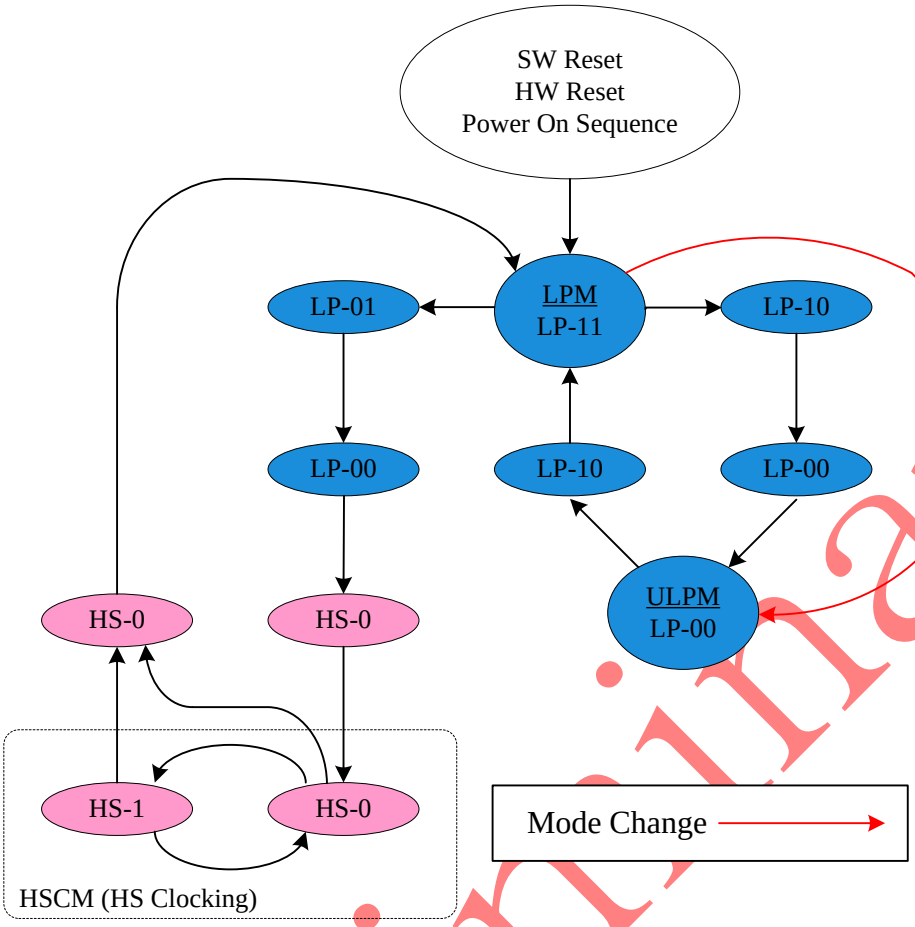
All Three Mode Changes to LPM on the Flow Chart

2. Ultra Low Power Mode (ULPM)



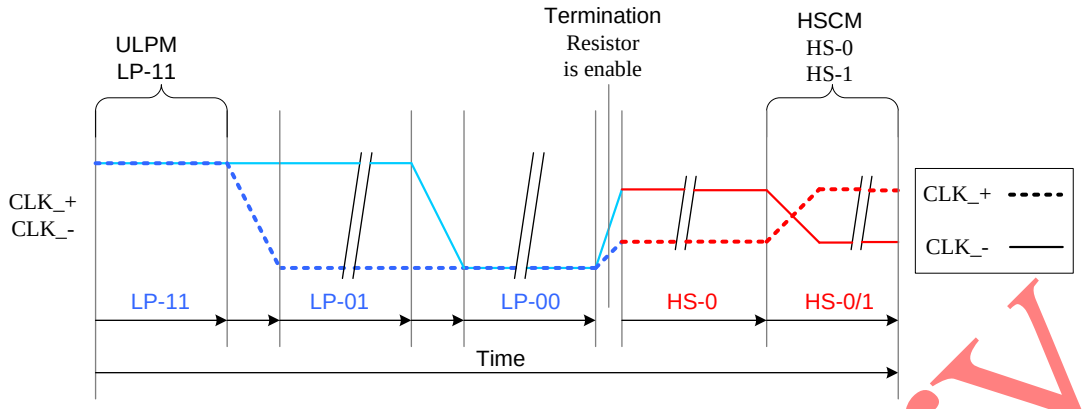
From LPM to ULPM

The mode change is also illustrated below.



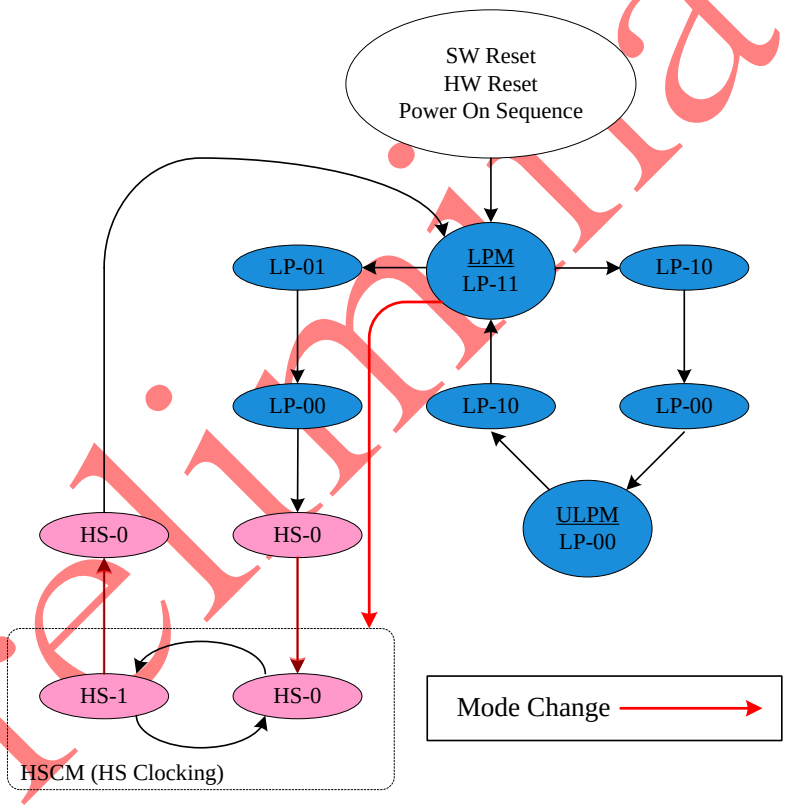
Mode Change from LPM to ULPM on the Flow Chart

3. High Speed Clock Mode (HSCM)



From LPM to HSCM

The mode change is also illustrated below.

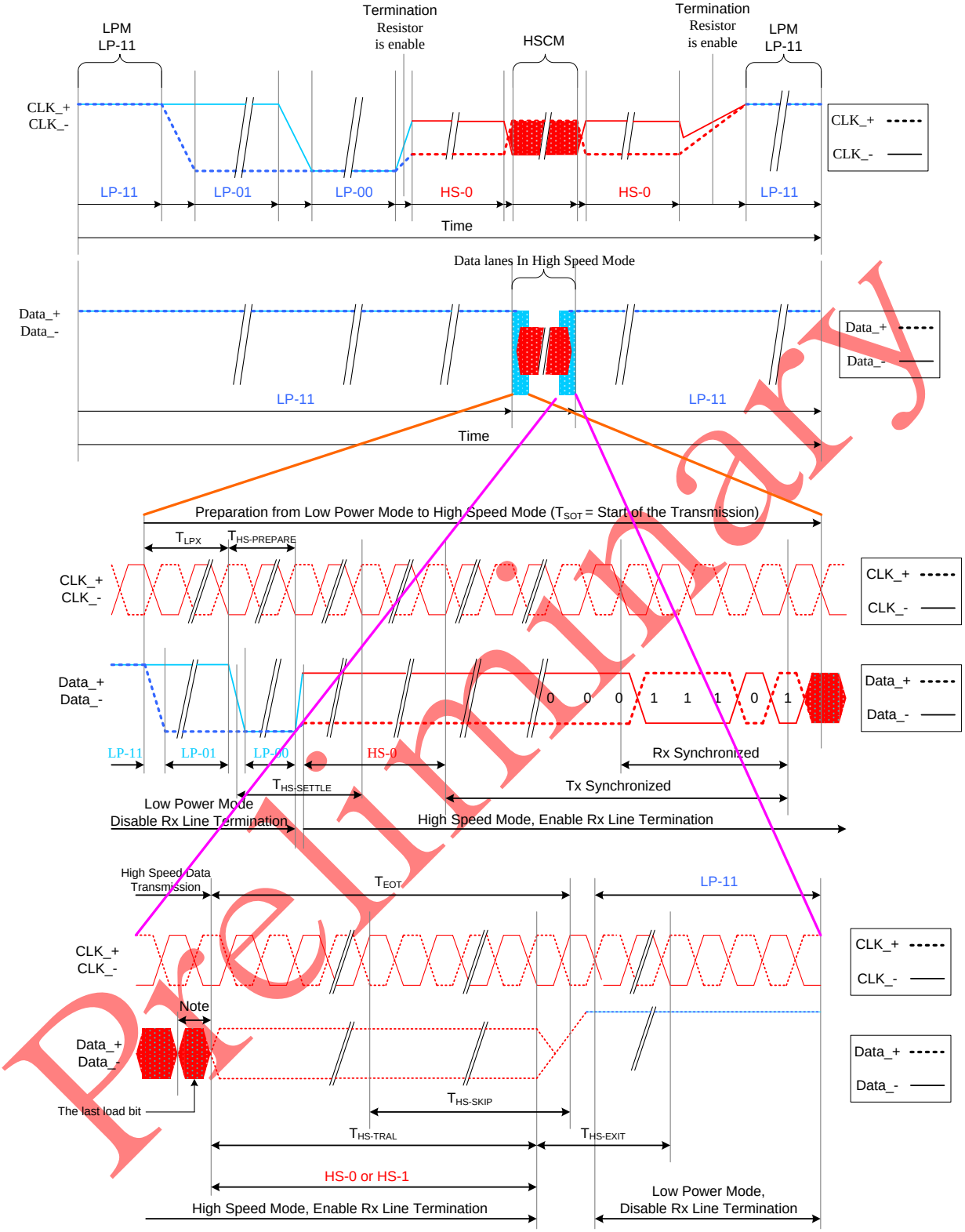


Mode Change from LPM to HSCM on the Flow Chart

The high speed clock (DSI-CLOCK_P/N) is started before high speed data is sent via DSI-DATA_P/N lanes. The high speed clock continues clocking after the high speed data sending has been stopped.

The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0



High Speed Clock Burst

Note:

If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1

If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0

8.10.1.4 DSI-DATA Lanes

DSI-DATA_P/N Data Lanes can be driven in different modes which are:

- Escape Mode
- High-Speed Data Transmission
- Bus Turnaround Request

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11=>LP-10=>LP-00=>LP-01=>LP-00	LP-00=>LP-10=>LP-11(Mark-1)
High-Speed Data Transmission	LP-11=>LP-01=>LP-00=>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11=>LP-10=>LP-00=>LP-10=>LP-00	High-Z, Note

1. **Escape Mode**

Data lanes (DSI-DATA_P/N) can be used in different Escape Modes when data lanes are in Low Power (LP) mode.

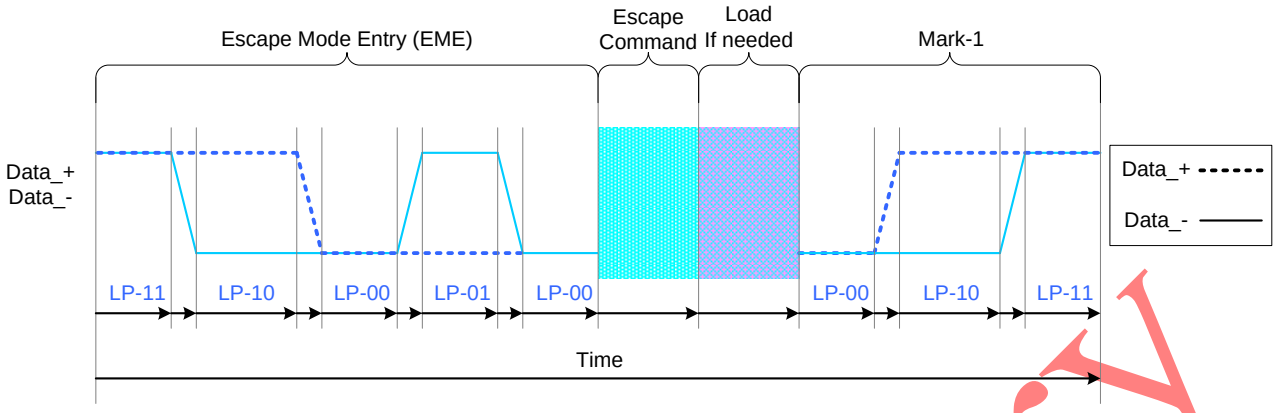
These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) e.g. from the MCU to the display module
- Drive data lanes to “Ultra-Low Power State” (ULPS)
- Indicate “Remote Application Reset” (RAR), which is reset the display module
- Indicate “Tearing Effect”, which is used for a TE line event from the display module to the MCU
- Indicate (ACK), which is used for a non-error event from the display module to the MCU

The basic sequence of the Escape Mode is as follow

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11
- End: LP-11

This basic construction is illustrated below:



General Escape Mode Sequence

The number of the different Escape Commands (EC) is eight. These eight different Escape Commands (EC) can be divided 2 different groups: Mode or Trigger. The MCU is informing to the display module that it is controlling data lanes (RX_D0P/N) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode. The MCU is waiting from the display module an event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

Escape commands are defined on the next table.

Escape command	Command Type Mode / Trigger	Entry command Pattern (First Last Bit Transmitted)
Low-Power Data	Mode	1110 0001 b
Ultra-Low Power Mode	Mode	0001 1110 b
Undefined-1, Note	Mode	1001 1111 b
Undefined-2, Note	Mode	1101 1110 b
Remote Application Reset	Trigger	0110 0010 b
Tearing Effect	Trigger	0101 1101 b
Acknowledge	Trigger	0010 0001 b
Uknown-5, Note	Trigger	1010 0000 b

Note: This Escape command support has not been implemented on the display module.

Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low Power Data Transmission (LPDT) is using a following sequence:

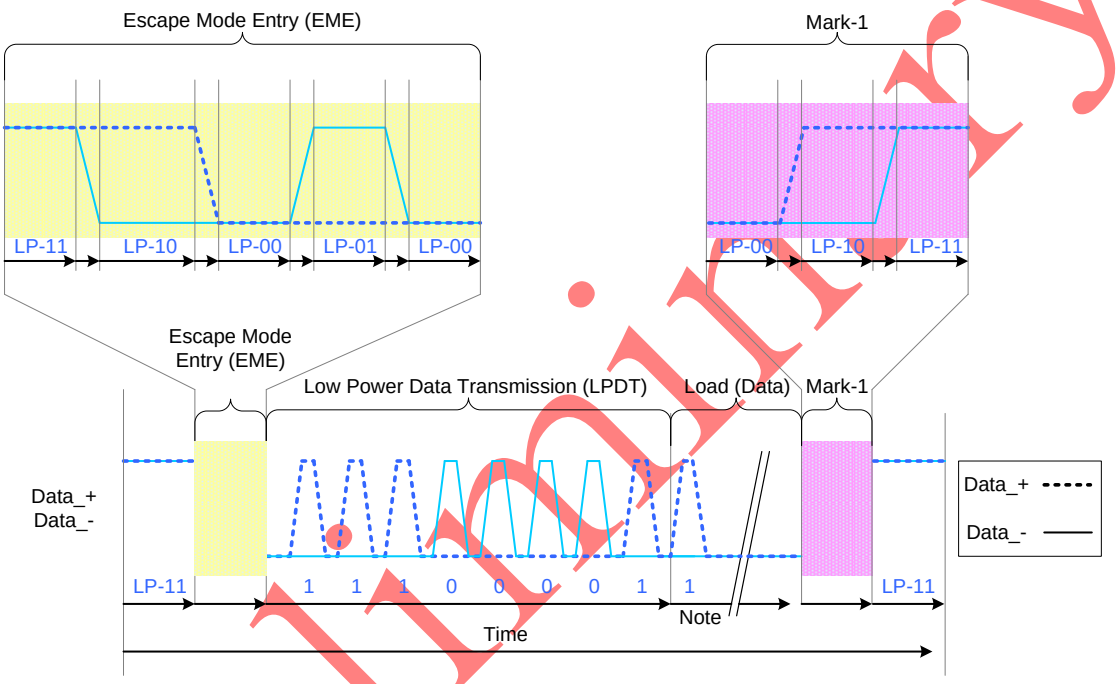
- Start: LP-11

- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Load (Data):

  One or more bytes (8 bit)

  Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

The Low-Power Data Transmission (LPDT) is as below,



Note : Load (Data) is presenting that the first bit is logical "1" in this Exsample

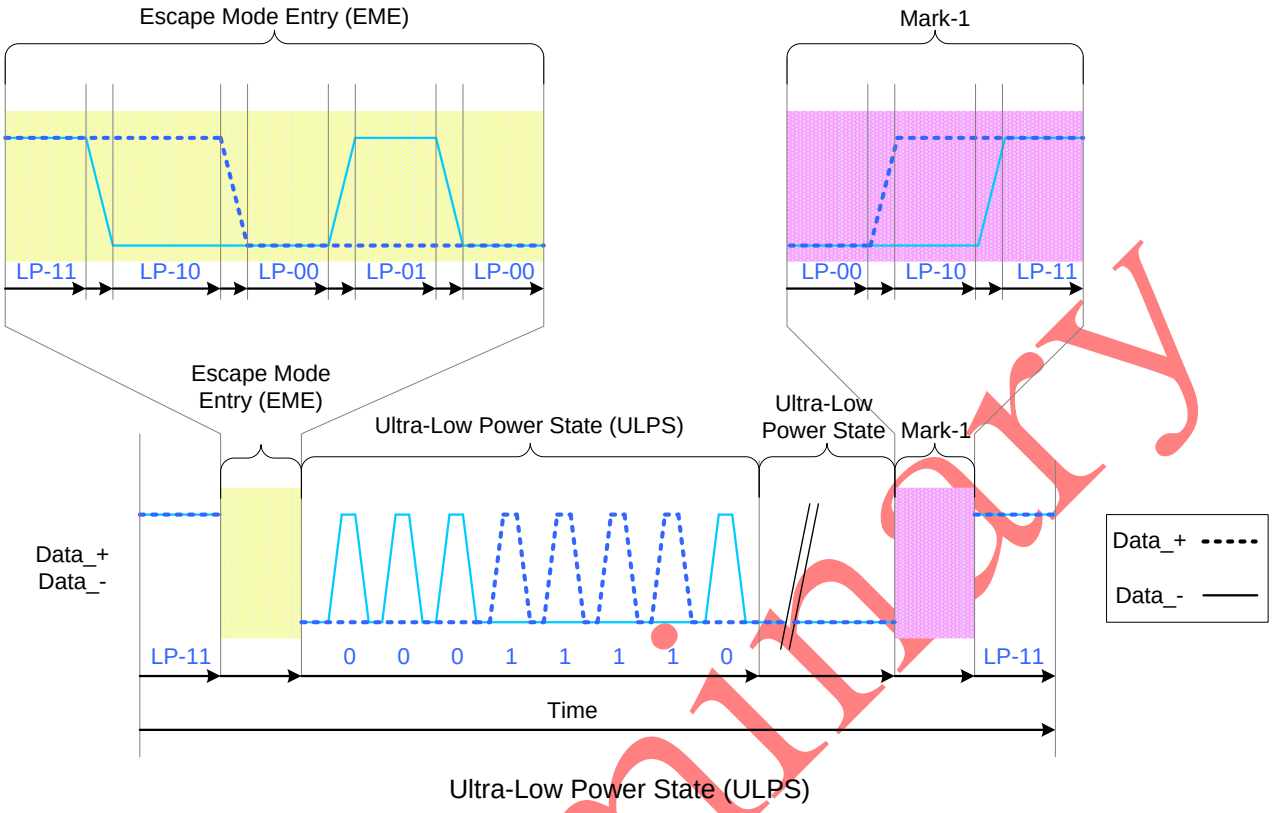
Low-Power Data Transmission (LPDT)

Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode. The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Ultra-Low Power State (ULPS)

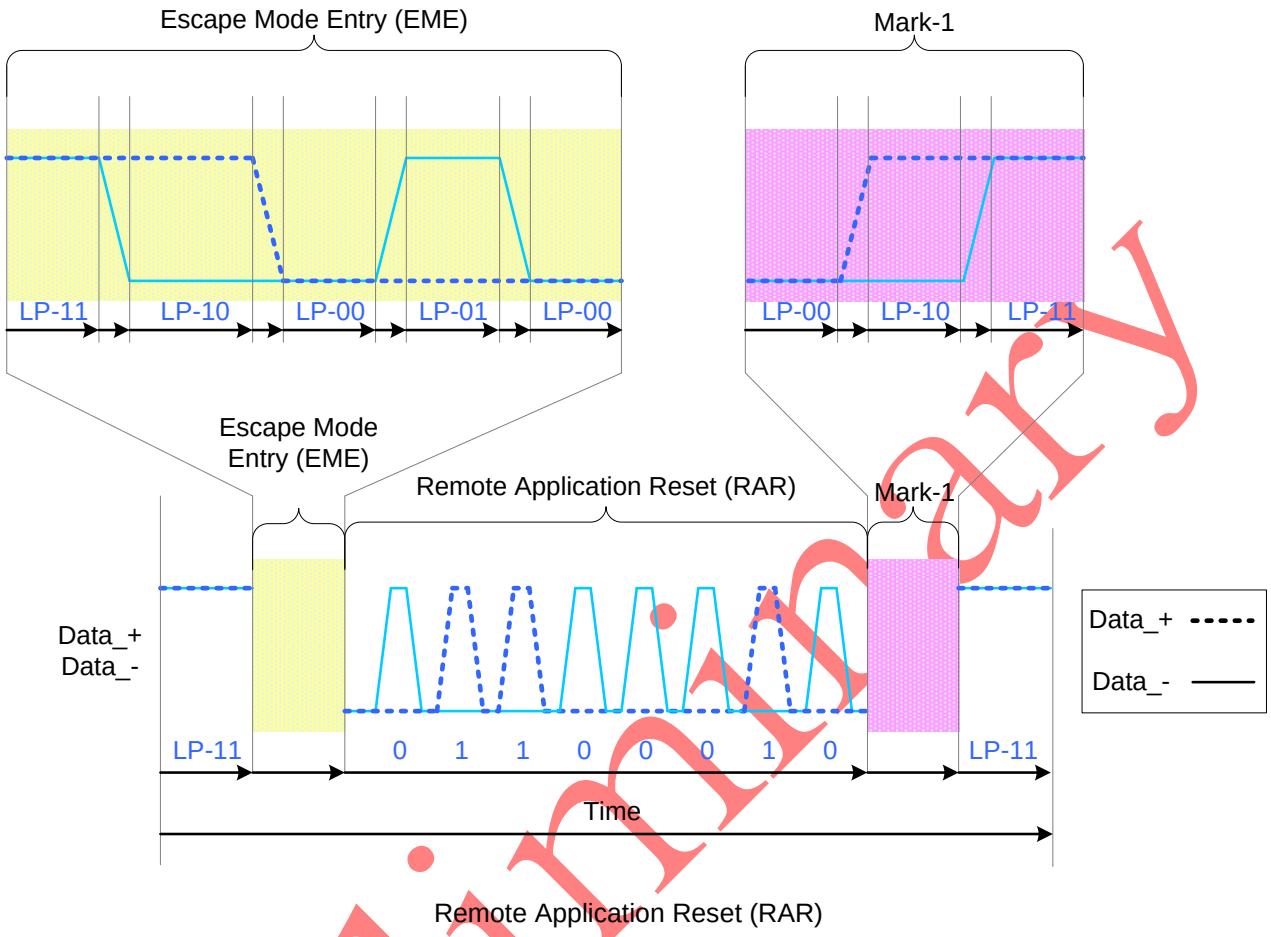
Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reseted in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



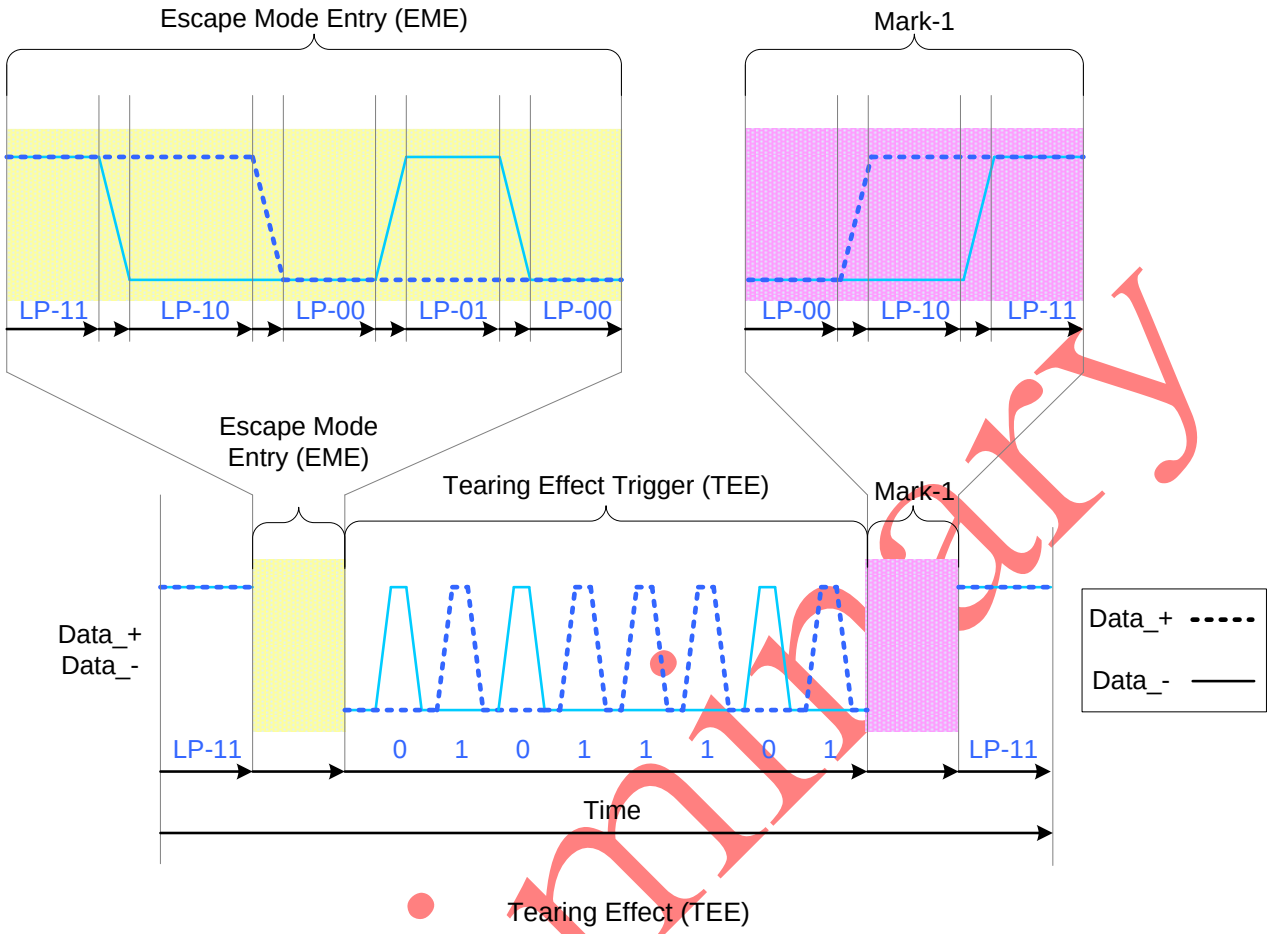
Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been appened on the display module by Tearing Effect (TEE).

The display module is sending the Tearing Effect (TEE) what is a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



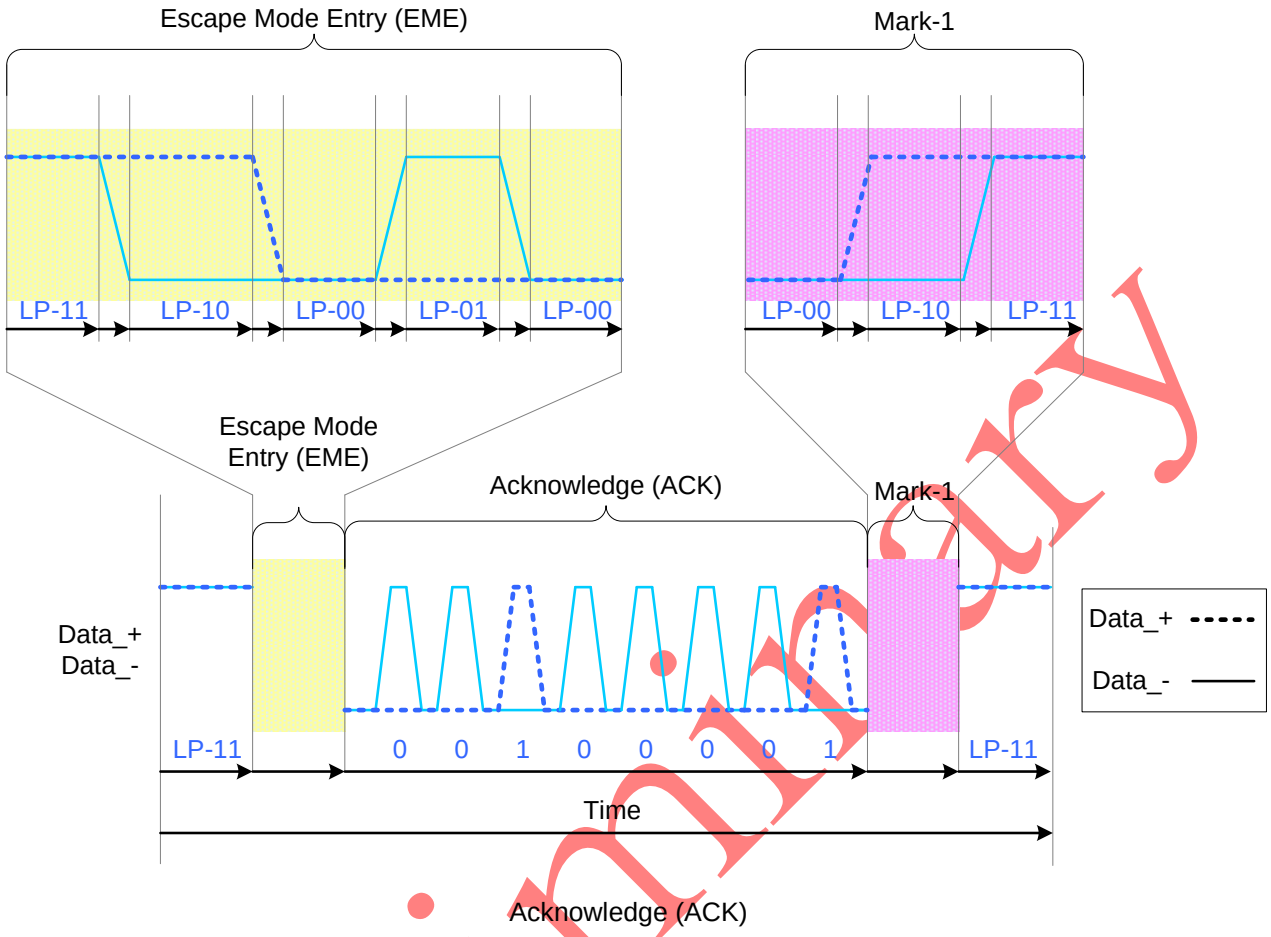
Acknowledge (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The display module is sending the Acknowledge (ACK) what is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



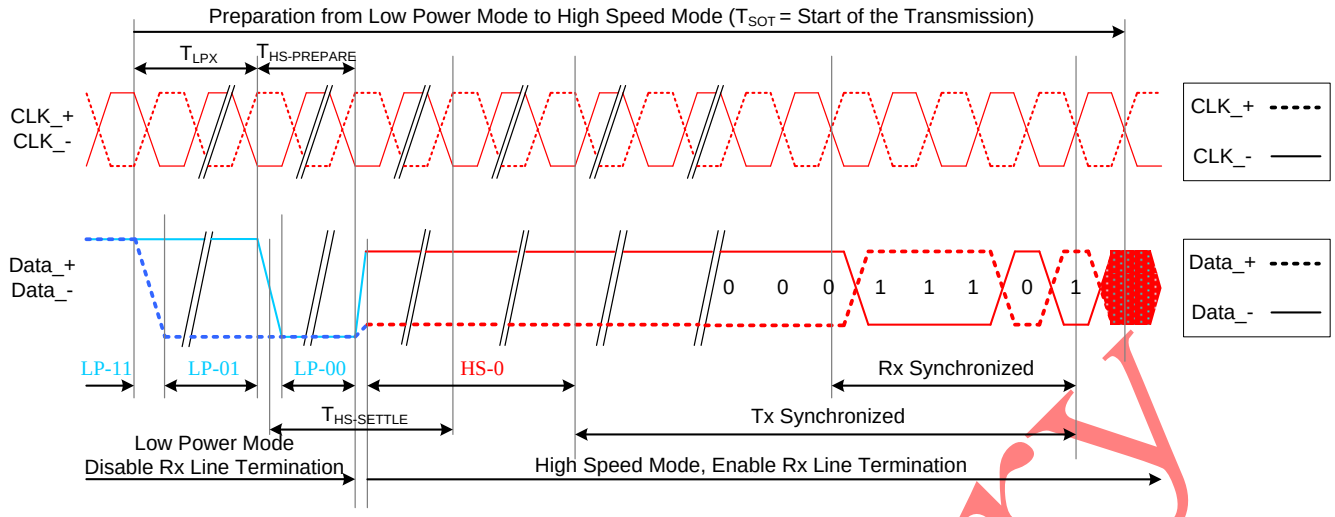
2. **High-Speed Data Transmission**

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes RX_CP/N have already been entered in the High-Speed Clock Mode (HSCM) by the MCU.

Data lanes of the display module are entering (T_{SOT}) in the High-Speed Data Transmission (HSDT) as follows:

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below



Entering High-Speed Data Transmission (T_{SOT} of HSDT)

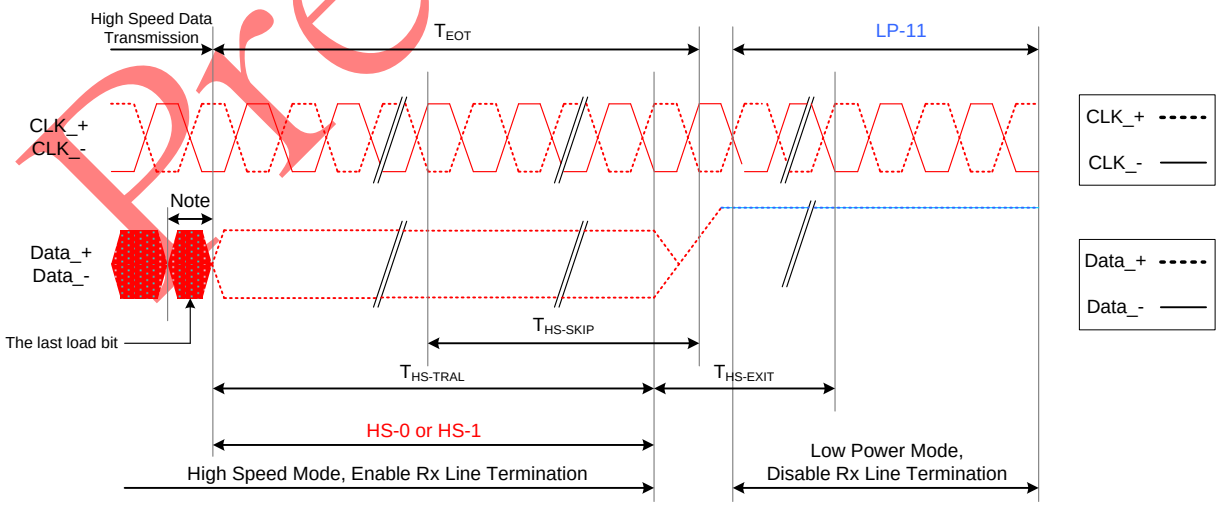
Leaving High-Speed Data Transmission

The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes RX_CP/N are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes are in LP-11 mode.

Data lanes of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows:

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
  - MCU changes to HS-1, if the last load bit is HS-0
  - MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below

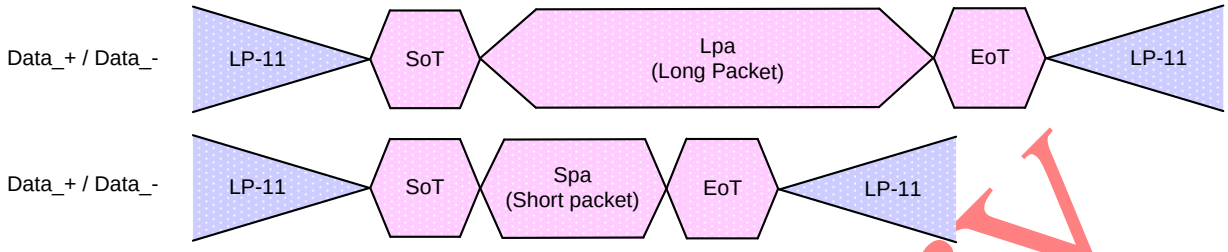


Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

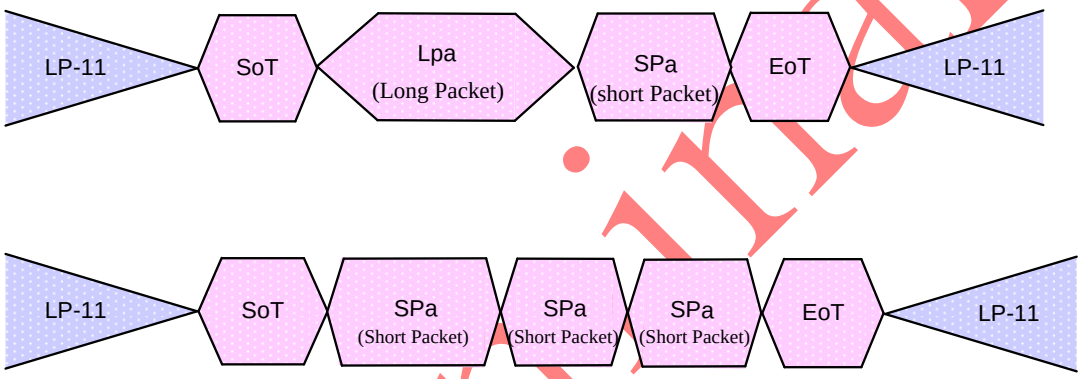
Burst of the High-Speed Data Transmission

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (Lpa) or Short (Spa) packets.

The single packet in High-Speed Data Transmission is illustrated for reference purposes below:

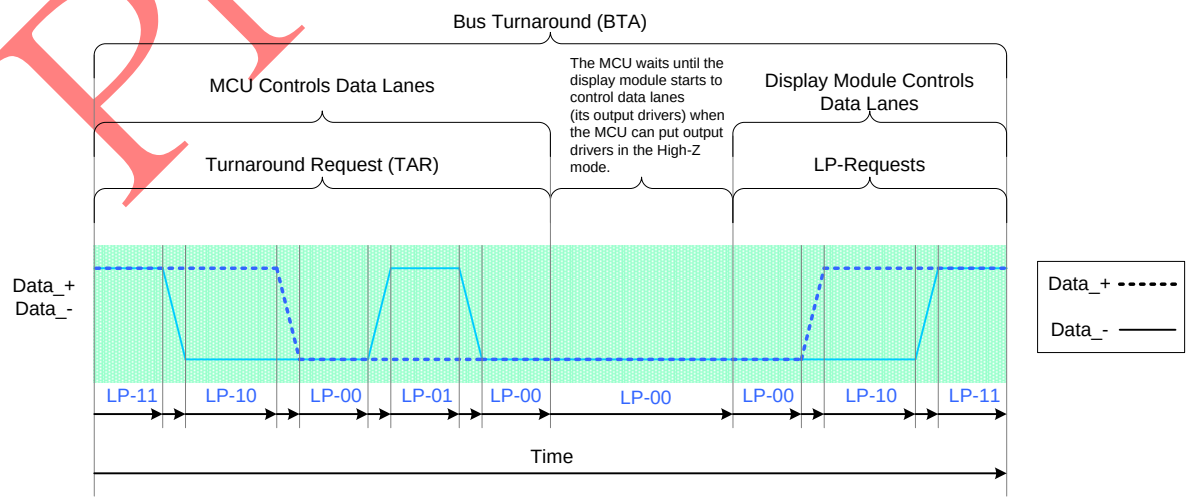


The multiple packets in High-Speed Data Transmission is illustrated for reference purposes below:



3. Bus Turnaround Request

The MCU which is controlling DSI-DATA_P/N Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or Display Module. The MCU and Display Module are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to Display Module, as follows.

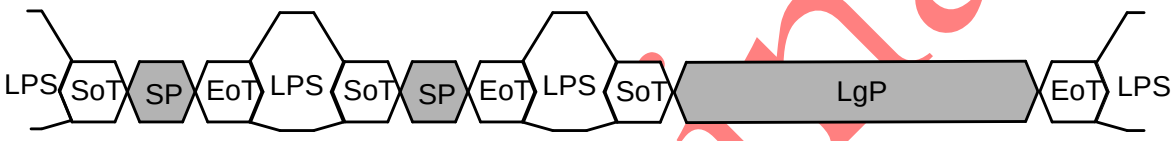


8.10.2 DSI protocol

The Protocol layer appends packet-protocol information and headers, and then sends complete bytes through the Lane Management layer to the PHY. Packets are serialized by the PHY and sent across the serial Link. The receiver side of a DSI Link performs the coverse of the transmitter side, decomposing the packet into parallel data, signal events and commands.

8.10.1.5 Multiple Packets per Transmission

There are two modes of data transmission, HS and LP transmission modes, at the PHY layer. Before a HS transmission can be started, the transmitter PHY issues a SoT sequence to the receiver. After that, data or command packets can be transmitted in HS mode. Multiple packets may exist within a single HS transmission and the end of transmission is always signaled at the PHY layer using a dedicated EoT sequence. In order to enhance the overall robustness of the system, DSI defines a dedicated EoT packet (EoTp) at the protocol layer for signaling the end of HS transmission. For backwards compatibility with earlier DSI systems, the capability of generating and interpreting this EoTp can be enabled or disabled.



Separate Transimssions

Key:

LPS -- Low power state
SoT -- Start of Transmission
EoT -- End of Transmission
SP -- Short Packet
LgP -- Long Packet

Single Transimssions

8.10.1.6 Packet Composition

The first byte of the packet, the Data Identifier (DI), includes information specifying the type of the packet. For example, in Video Mode systems in a display application the logical unit for a packet may be one horizontal display line. Command Mode systems send commands and an associated set of parameters, with the number of parameters depending on the command type.

Packet sizes fall into two categories:

- **Short packets** are four bytes in length including the ECC. Short packets are used for most Command Mode commands and associated parameters. Other Short packets convey events like H Sync and V Sync edges. Because they are Short packets they can convey accurate timing information to logic at the peripheral.
- **Long packets** specify the payload length using a two-byte Word Count field. Payloads may be

from 0 to 2^{16}-1 bytes long. Therefore, a Long packet may be up to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data.

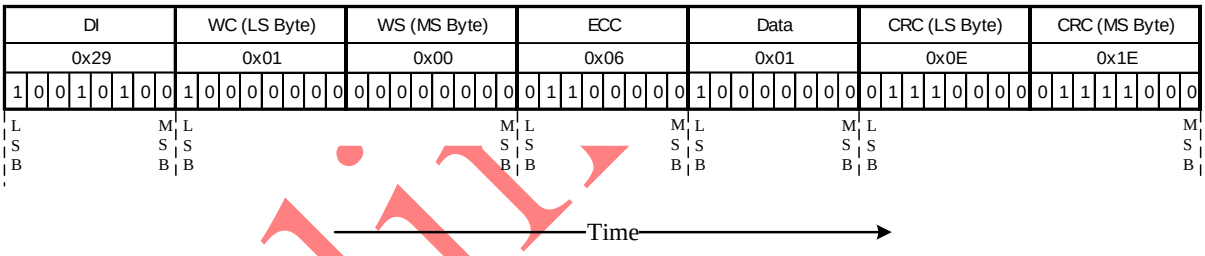
A special case of Command Mode operation is video-rate (update) streaming, which takes the form of an arbitrarily long stream of pixel or other data transmitted to the peripheral. As all DSI transactions use packets, the video stream shall be broken into separate packets. This “packetization” may be done by hardware or software. The peripheral may then reassemble the packets into a continuous video stream for display.

The Set Maximum Return Packet Size command allows the host processor to limit the size of response packets coming from a peripheral.

8.10.1.7 Endian Policy

All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified.

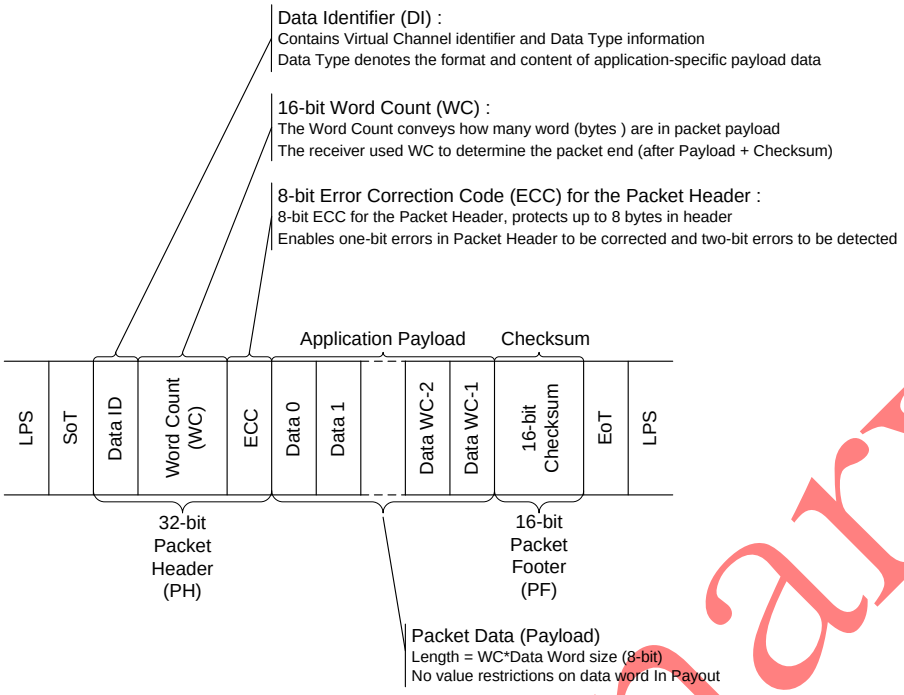
Figure 12 shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.



Endian Example (Long Packet)

8.10.1.8 General Packet Structure(Long Packet Format)

A Long packet shall consist of three elements: a 32-bit Packet Header (PH), an application-specific Data Payload with a variable number of bytes, and a 16-bit Packet Footer (PF). The Packet Header is further composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.



Long Packet Structure

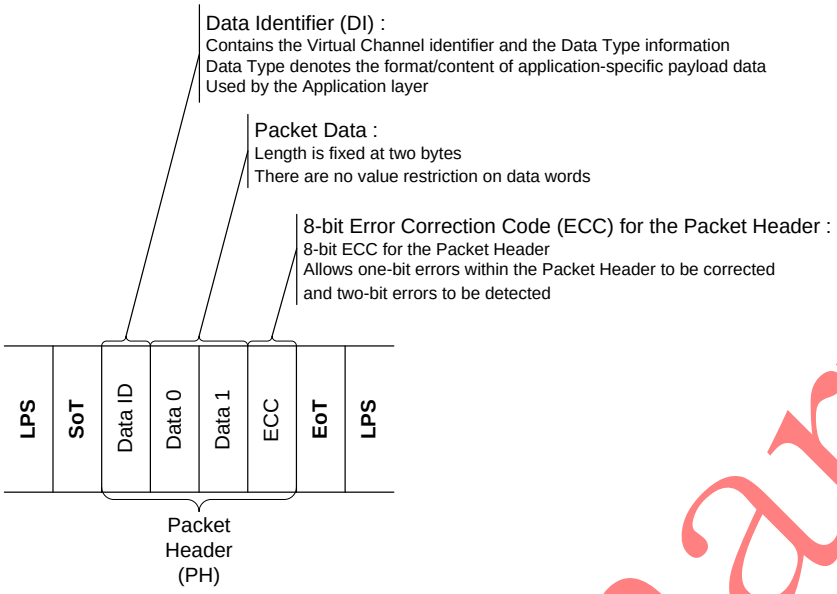
The Data Identifier defines the Virtual Channel for the data and the Data Type for the application specific payload data. See sections 8.8 through 8.10 for descriptions of Data Types. The Word Count defines the number of bytes in the Data Payload between the end of the Packet Header and the start of the Packet Footer. Neither the Packet Header nor the Packet Footer shall be included in the Word Count. The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. This includes both the Data Identifier and Word Count fields. After the end of the Packet Header, the receiver reads the next Word Count * bytes of the Data Payload. Within the Data Payload block, there are no limitations on the value of a data word, i.e. no embedded codes are used. Once the receiver has read the Data Payload it reads the Checksum in the Packet Footer. The host processor shall always calculate and transmit a Checksum in the Packet Footer. Peripherals are not required to calculate a Checksum. Also note the special case of zero-byte Data Payload: if the payload has length 0, then the Checksum calculation results in (FFFFh). If the Checksum is not calculated, the Packet Footer shall consist of two bytes of all zeros (0000h). See section 9 for more information on calculating the Checksum. In the generic case, the length of the Data Payload shall be a multiple of bytes. In addition, each data format may impose additional restrictions on the length of the payload data, e.g. multiple of four bytes. Each byte shall be transmitted least significant bit first. Payload data may be transmitted in any byte order restricted only by data format requirements. Multi-byte elements such as Word Count and Checksum shall be transmitted least significant byte first

.

8.10.1.9 General Packet Structure(Short Packet Format)

A Short packet shall contain an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC; a Packet Footer shall not be present. Short packets shall be four bytes in length. The Error Correction Code

(ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Short packet.



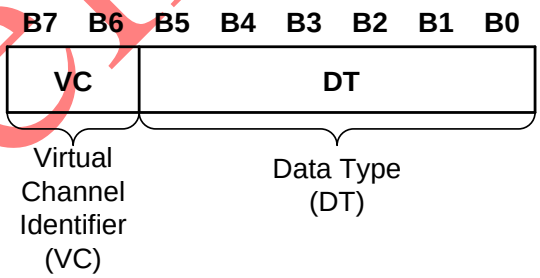
Short Packet Structure

8.10.1.10 Common Packet Elements

Long and Short packets have several common elements that are described in this section.

➢Data Identifier Byte

The first byte of any packet is the DI (Data Identifier) byte. Figure 15 shows the composition of the Data Identifier (DI) byte. DI[7:6]: These two bits identify the data as directed to one of four virtual channels.DI[5:0]: These six bits specify the Data Type.

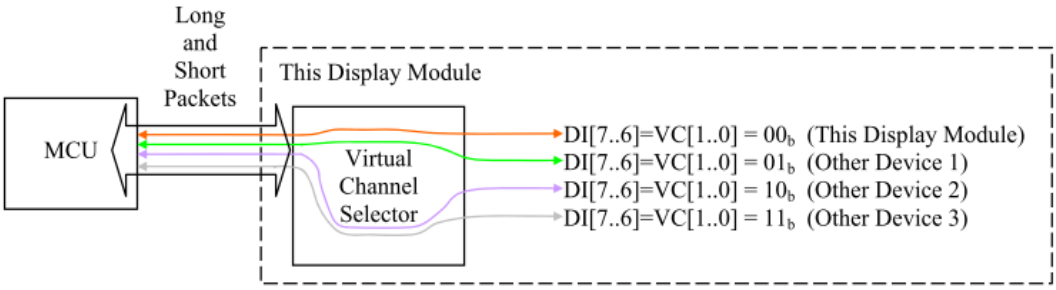


Data Identifier Byte

Virtual Channel Identifier – VC field, DI[7:6]

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals. The Virtual Channel ID enables one serial stream to service two or more virtual peripherals by multiplexing packets onto a common transmission channel. Note that packets sent in a single transmission each have their own Virtual Channel assignment and can be directed to different peripherals. Although the DSI protocol permits communication with multiple peripherals, this specification only addresses the connection of a host processor to a single peripheral. Implementation details for connection to more than one physical peripheral are beyond the scope

of this document.



Virtual Channel (VC) Configuration

Data Type Field DT[5:0]

The Data Type field specifies if the packet is a Long or Short packet type and the packet format. The Data Type field, along with the Word Count field for Long packets, informs the receiver of how many bytes to expect in the remainder of the packet. This is necessary because there are no special packet start / end sync codes to indicate the beginning and end of a packet. This permits packets to convey arbitrary data, but it also requires the packet header to explicitly specify the size of the packet. When the receiving logic has counted down to the end of a packet, it shall assume the next data is either the header of a new packet or the EoT (End of Transmission) sequence.

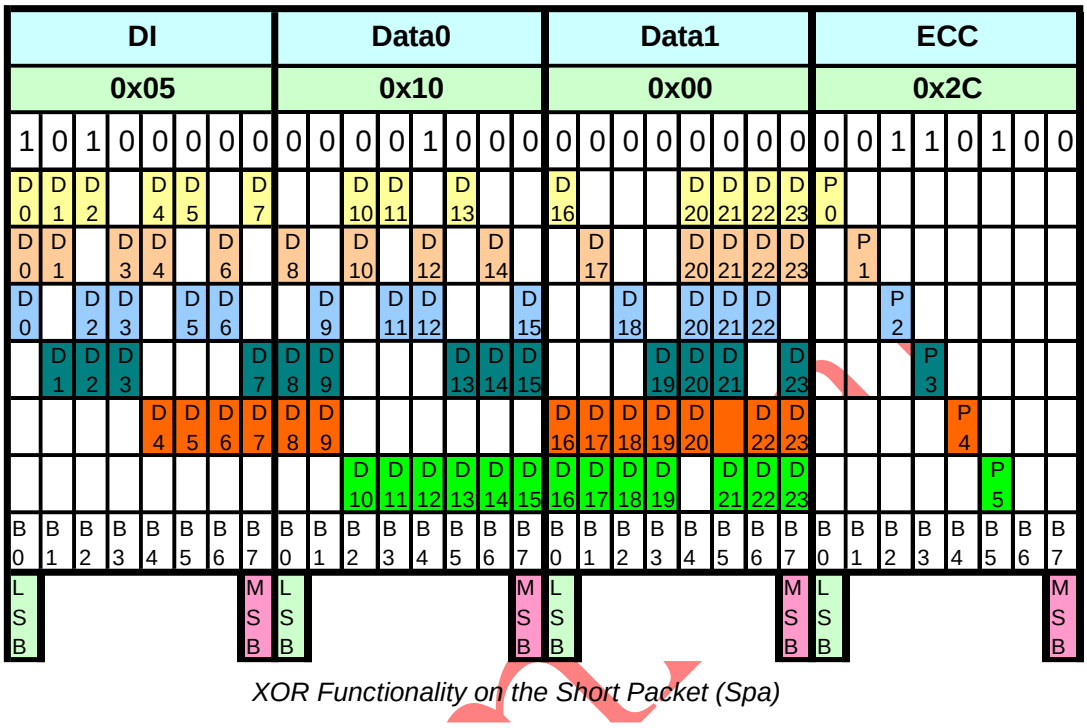
8.10.1.11 Error Correction Code

The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. The host processor shall always calculate and transmit an ECC byte. Peripherals shall support ECC in both forward- and reverse-direction communications.

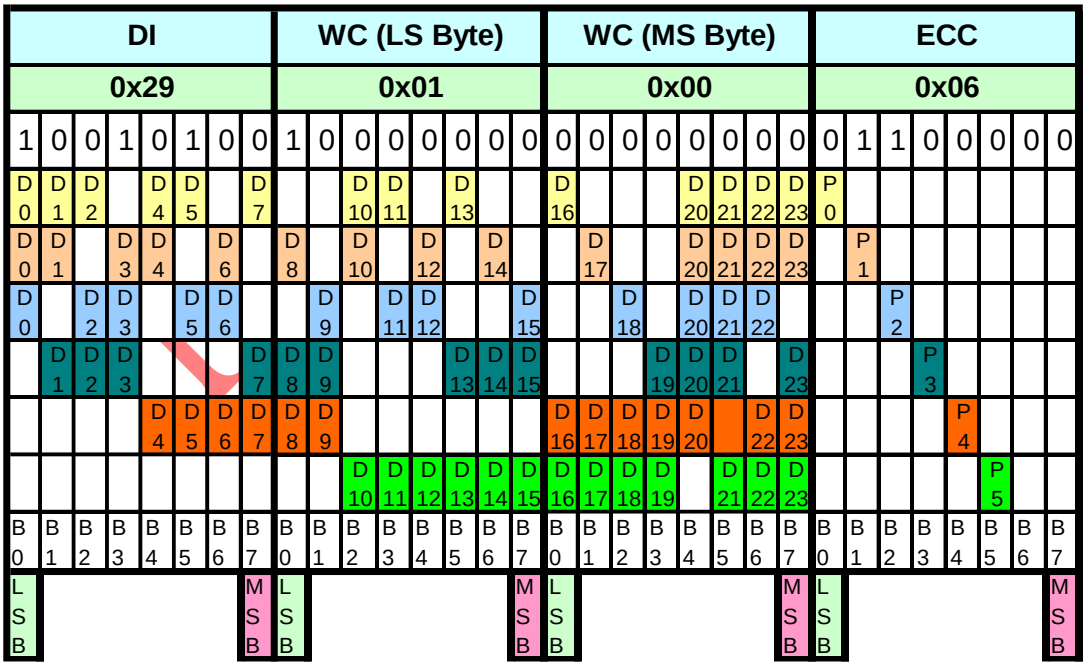
Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

P7 = 0
P6 = 0
P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to ‘0’ because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D [23…0]). Therefore, there is only needed 6 bits (P [5…0]) for Error Correction Code (ECC).



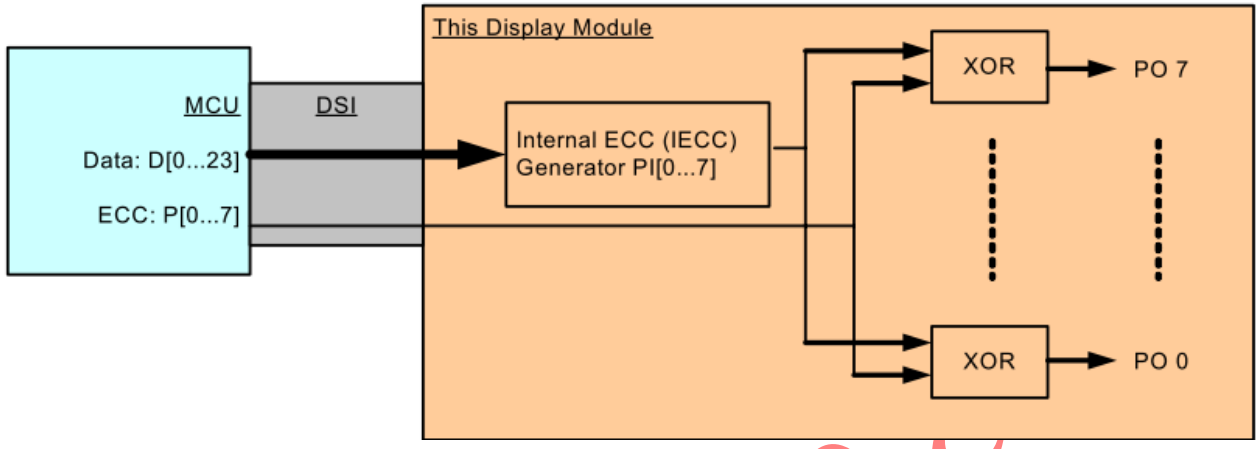
XOR Functionality on the Short Packet (Spa)



XOR Functionality on the Long Packet (Lpa)

The transmitter (The MCU or the Display Module) is sending data bits D[23:0] and Error Correction Code (ECC) P[7:0]. The receiver (The Display module or the MCU) is calculate an Internal Error Correction

Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7:0].



Internal Error Correction Code (IECC) on the Display Module (The Receiver)

The sent data bits (D[23:0]) and ECC (P[7:0]) are received correctly, if a value of the PO[7:0]) is 00h. The sent data bits (D[23:0]) and ECC (P[7:0]) are not received correctly, if a value of the PO[7:0]) is not 00h.

ECC P[7:0]	1	1	0	0	0	0	0	0	03h
IECC PI[7:0]	1	1	0	0	0	0	0	0	03h
XOR(ECC,IECC	0	0	0	0	0	0	0	0	=00h => No Error
	L							M	
	S							S	
	B							B	

Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7:0]	1	1	0	0	0	0	0	0	03h
IECC PI[7:0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC,IECC	0	0	1	1	0	0	0	0	=0Ch => Error
	L							M	
	S							S	
	B							B	

Internal XOR Calculation between ECC and IECC Values – Error

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

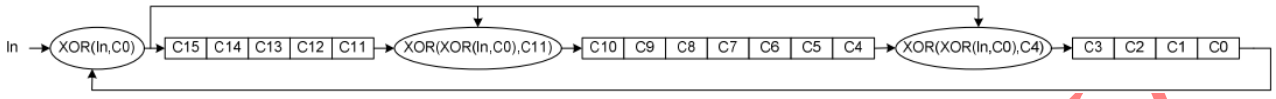
One error is detected if the value of the PO[7:0] is on the above table : One it Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

- PO [7…0] = 0Eh
- The bit of the data (D [23:0]), what is not correct, is D[3]

More than one error is detected if the value of the PO [7…0] is not on the above table: One Bit Error Value of the Error Correction Code (ECC) e.g. PO [7…0] = 0Ch.

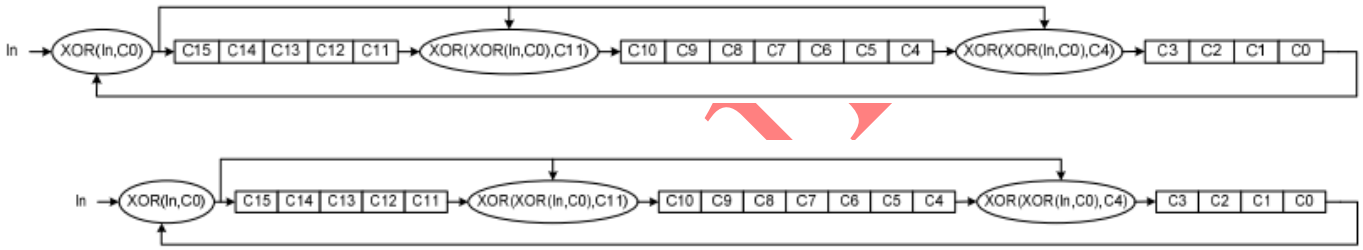
8.10.1.12 Packet Footer on the Long Packet

Packet Footer (PF) of the Long Packet (Lpa) is defined after the Packet Data (PD) of the Long Packet (Lpa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (Lpa). The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial $X_{16} + X_{12} + X_5 + X_0$ as it is illustrated below.



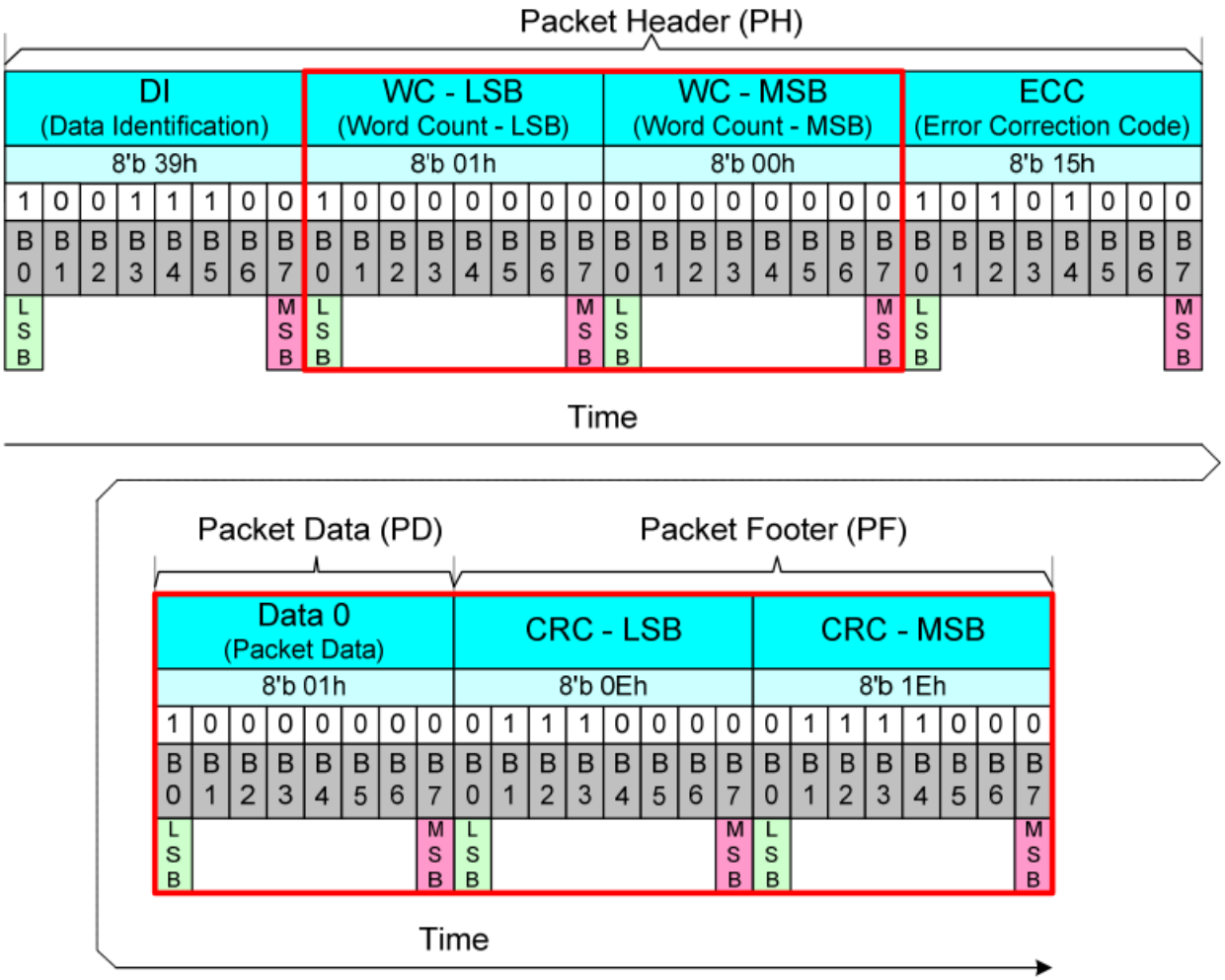
The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (Lpa) is 01h, is illustrated (step-by-step) below.



Step	In	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11(Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4(Step-1))	C3	C2	C1	C0	C0
0	X	X	1	1	1	1	1	X	1	1	1	1	1	1	1	X	1	1	1	1	X
1	1(LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
8	0(MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
	1 byte	CRC result	0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0	
			MSB																	LSB	

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.



The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) is equal and vice versa the received Packet Data (PD) and Packet Footer(PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

8.10.1.13 Processor to Peripheral Direction Packet Data Types

The set of transaction types sent from the host processor to a peripheral, such as a display module, are show as below table.

Data type	Data type, binary	Description packet	Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of Transmission packet (EoTp)	Short
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short
22h	10 0010	Shut Down Peripheral Command	Short
32h	11 0010	Turn On Peripheral Command	Short
03h	00 0011	Generic Short WRITE, no parameters	Short
13h	01 0011	Generic Short WRITE, 1 parameter	Short
23h	10 0011	Generic Short WRITE, 2 parameters	Short
04h	00 0100	Generic READ, no parameters	Short
14h	01 0100	Generic READ, 1 parameter	Short
24h	10 0100	Generic READ, 2 parameters	Short
05h	00 0101	DCS Short WRITE, no parameters	Short
15h	01 0101	DCS Short WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
X0h / XFh, unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	

Data Types for Processor-sourced Packets

All detail function of data types is as below：

Sync event (H Start, H End, V Start, V End), Data Type = xx 0001 (x1h)

Sync event (H start, H end, V start, V end), data type=xx 0001 (x1h)		
Data type, hex	**Function description**	**Number of bytes**
01h	Sync Event, V Sync Start	Short
11h	Sync Event, V Sync End	Short
21h	Sync Event, H Sync Start	Short
31h	Sync Event, H Sync End	Short
Note: In order to represent timing information as accurately as possible a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Similarly, a V Sync End event implies an H Sync Start event for the last line of the VSA.		

Color mode status (Color Mode On, Color Mode Off)		
Data type, hex	**Function description**	**Number of bytes**
02h	Color Mode On that switches a Video Mode display module to a low-color mode for power saving.	Short
12h	Color Mode Off that switches a Video Mode display module from low-color display to normal display.	Short

Display status (shutdown command, turn-on command)		
Data type, hex	**Function description**	**Number of bytes**
22h	Shutdown Peripheral command that turns off the display in a Video Mode display for power saving.	Short
32h	Turn On Peripheral command that turns on the display in Video Mode display for normal display.	Short
Note: When use shutdown command, interface shall remain powered in order to receive the turn-on, or wake-up, command.		

DCS command setting		
Data type, hex	**Function description**	**Number of bytes**
05/15h	DCS Short Write command is used to write a single data byte to a peripheral such as a display module. If a parameter is not required, the parameter byte shall be 00h.	Short
06h	DCS Read command, the returned data may be of Short or Long packet format.	Short

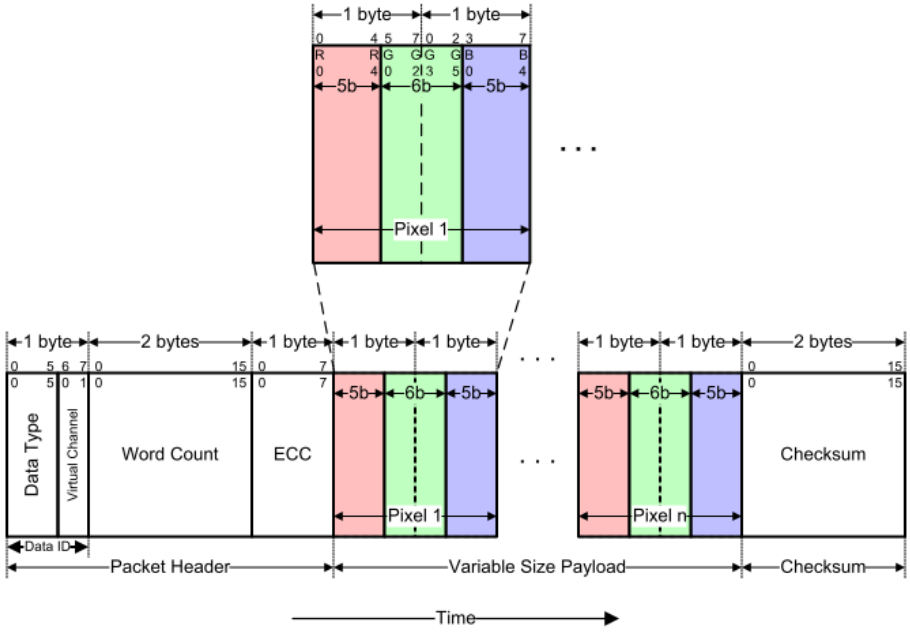
39h	DCS Long Write/ Write _ LUT Command is used to send larger blocks of data to a display module that implements the Display Command Set.	Long

Return packet size setting		
Data type, hex	**Function description**	**Number of bytes**
37h	Set Maximum Return Packet Size that specifies the maximum size of the payload in a Long packet transmitted from peripheral back to the host processor.	Short
Note: The two-byte value is transmitted with LS byte first. And during a power-on or Reset sequence, the Maximum Return Packet Size shall be set by the peripheral to a default value of one.		

Variable data packet		
Data type, hex	**Function description**	**Number of bytes**
09h	Null Packet is a mechanism for keeping the serial Data Lane(s) in High-Speed mode while sending dummy data.	Short
19h	Blanking packet is used to convey blanking timing information in a Long packet.	Short
Note: (1) When Null Packet, the Payload Data belong “null” Data, actual data values sent are irrelevant because the peripheral does not capture or store the data. (2) When Blanking packet, the packet represents a period between active scan lines of a Video Mode display,		

Data stream format – 16bit Format

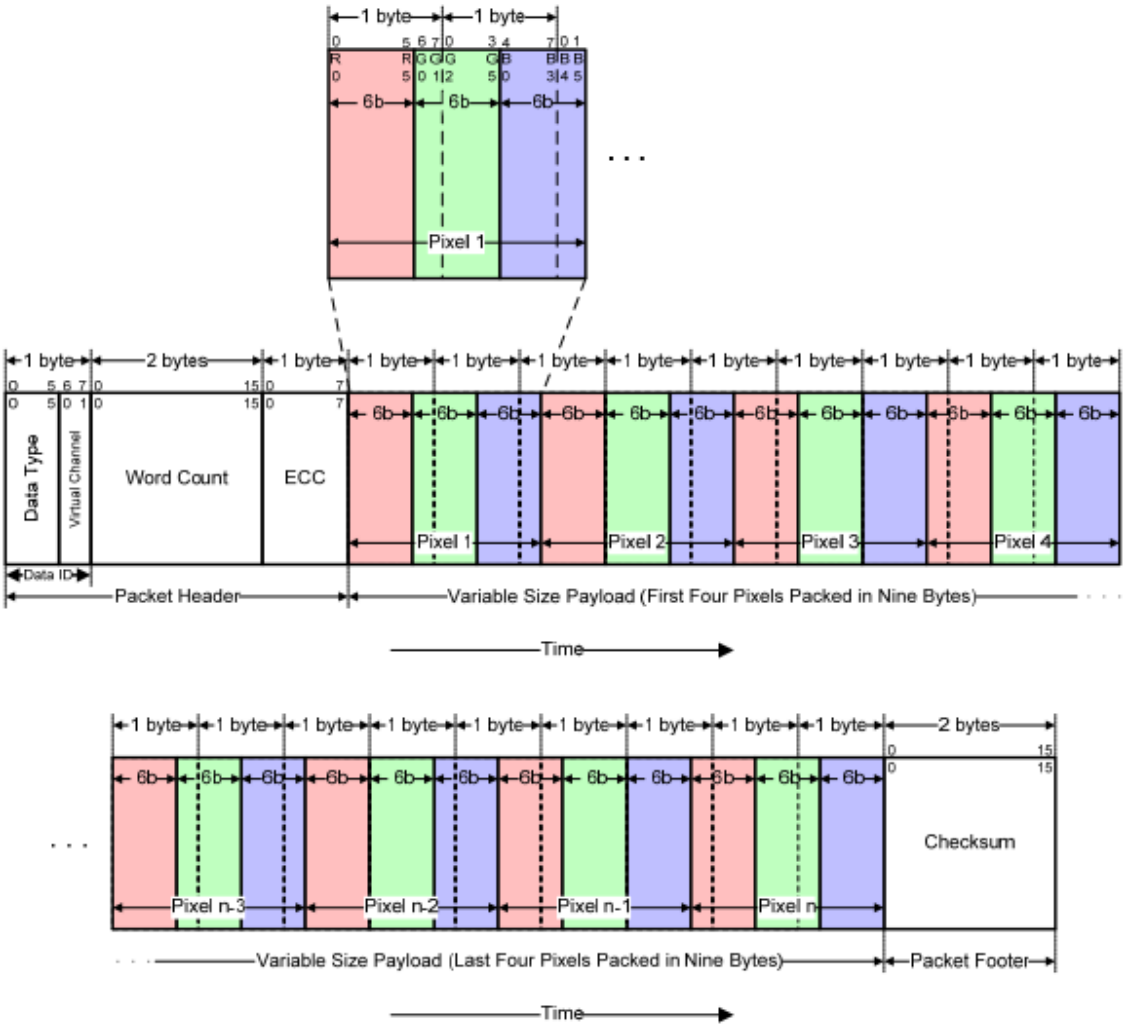
Data stream format – 16bit Format		
Data type, hex	**Function description**	**Number of bytes**
0Eh	Packed Pixel Stream 16-Bit Format is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. Pixel format is five bits red, six bits green, five bits blue, in that order.	Long



Note: That the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.

Data stream format – 18bit Format (mode1)

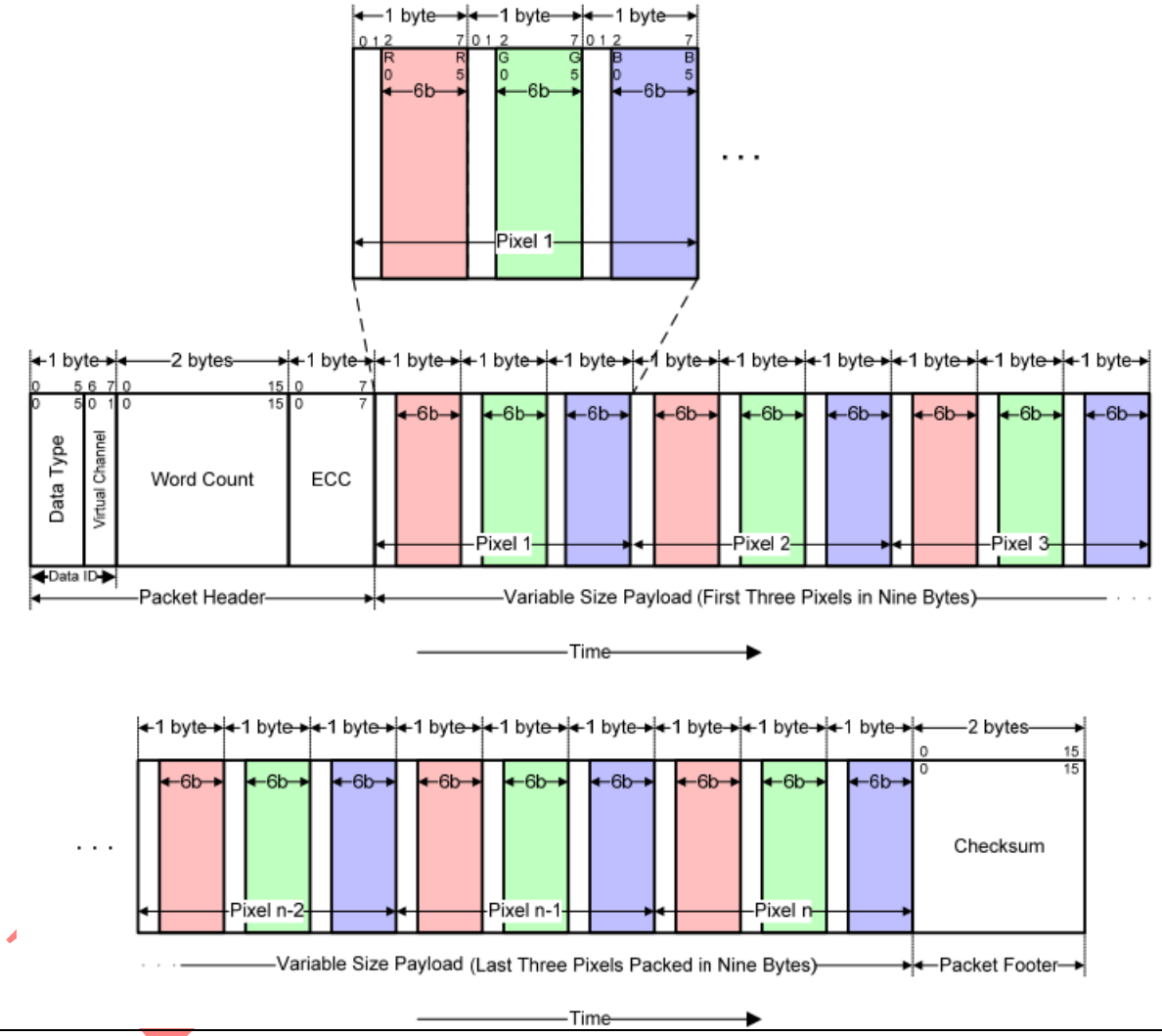
Data stream format – 18bit Format(Mode1)		
Data type, hex	**Function description**	**Number of bytes**
1Eh	Packed Pixel Stream 18-Bit Format is a Long packet used to transmit image data formatted as 18-bit pixels to a Video Mode display module. Pixel format is six bits red, six bits green, six bits blue, in that order.	Long



Note: Within a color component, the LSB is sent first and the MSB last and pixel boundaries only line up with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. It is possible to send pixel data that represent a line width that is not a multiple of four pixels, but display logic on the receiver end shall dispose of the extra bits of the partial byte at the end of active display and ensure a “clean start” for the next line.

Data stream format – 18bit Format(mode2)

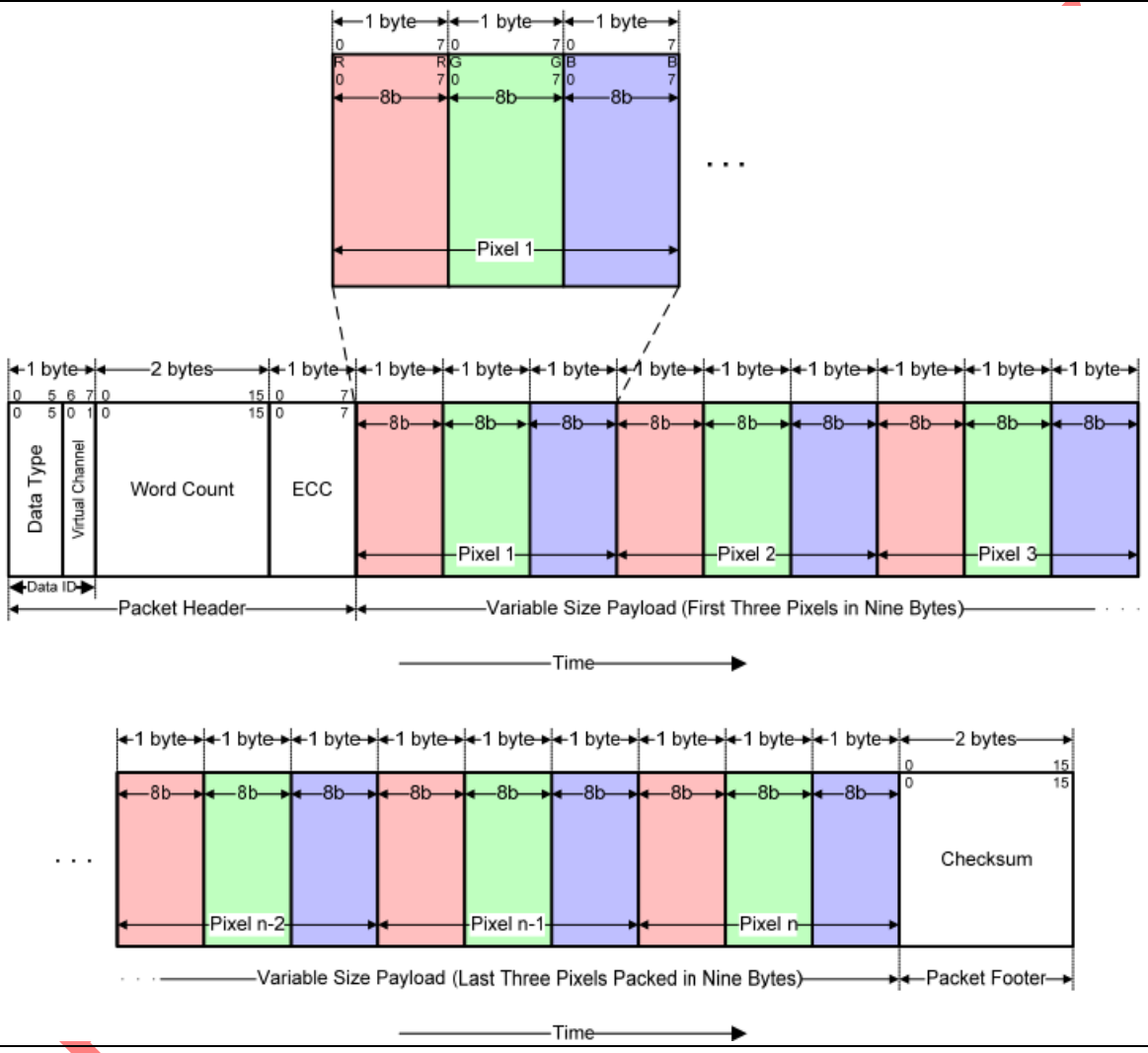
Data stream format – 18bit Format(Mode2)		
Data type, hex	**Function description**	**Number of bytes**
2Eh	In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits[1:0] of each payload byte representing active pixels are ignored.	Long



Note: Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

Data stream format – 24bit Format

Data stream format –24bit Format		
Data type, hex	**Function description**	**Number of bytes**
3Eh	Packed Pixel Stream 24-Bit Format is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. Pixel format is (8 bits) red, (8 bits) green and (8 bits) blue.	Long



Note: Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

8.10.1.14 Peripheral-to-Processor (Reverse Direction) LP Transmissions

All Command Mode systems require bidirectional capability for returning READ data, acknowledge, or error information to the host processor. Multi-Lane systems shall use Lane 0 for all peripheral-to-processor transmissions; other Lanes shall be unidirectional. Reverse-direction signaling shall only use LP (Low Power) mode of transmission.

Peripheral-to-processor transactions are of four basic types:

- Tearing Effect is a Trigger message sent to convey display timing information to the host processor. Trigger messages ate signal byte packets sent by a peripheral's PHY layer in response to a signal form the DSI protocol layer.
- Acknowledge is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication.
- Acknowledge and Error Report is a Short packet sent if any errors were detected in preceding transmission from the host processor. Once reported, accumulated errors in the error register are cleared.
- Response to Read Request may be Short or Long packet that returns data requested by the preceding READ command from the processor.

In general, if the host processor completes a transmission to the peripheral with BTA asserted, the peripheral shall respond with one or more appropriate packet(s), and then return bus ownership to the host processor. If BTA is not asserted following a transmission from the host processor, the peripheral shall not communicate an Acknowledge or error information back to the host processor.

Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected responses, are as follows:

- Following a non-Read command in which no error was detected, the peripheral shall respond with Acknowledge.
- Following a Read request in which no error was detected, the peripheral shall send the requested READ data.
- Following a Read request in which the ECC error was detected and corrected, the Peripheral shall send the requested READ data in a Long or Short packet, followed by a 4-byte (Acknowledge with Error Report) packet in the same LP transmission. The Error Report shall have the ECC Error flag set.
- Following a non-Read command in which the ECC error was detected and corrected, the peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte (Acknowledge with Error Report) packet, the Error Report shall have the ECC Error flag set.
- Following any command in which SoT Error, SoT Sync Error, EoT Sync Error, LP Transmit Sync Error, checksum error or DSI VC ID Invalid was detected, or the DSI command was not

recognized, the peripheral shall send a 4-byte Acknowledge with Error Report response, with the appropriate error flags set in the two-byte error field. Only the ACK/Error Report packet shall be transmitted; no read or write accesses shall take place on the peripheral in response.

An error report is a Short packet comprised of two bytes following the DI byte, with an ECC byte following the Error Report bytes. By convention, detection and reporting of each error type is signified by setting the corresponding bit to “1”. Table 18 shows the bit assignment for all error reporting.

Bit	Error Report Bit Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	HS Receive Timeout Error
6	False Control Error
7	Reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Invalid Transmission Length
14	Reserved
15	DSI Protocol Violation

The table as below presents the complete set of peripheral-to-processor Data Types

Data type, hex	Data type, binary	Description packet	Size
02h	00 0010	Acknowledge and Error Report	Short
08h	00 1000	End of Transmission packet (EoTp)	Short
11h	01 0001	Generic Short READ Response, 1 byte returned	Short
12h	01 0010	Generic Short READ Response, 2 bytes returned	Short
1Ah	01 1010	Generic Long READ Response	Short
1Ch	01 1100	DCS Long READ Response	Short
21h	10 0001	DCS Short READ Response, 1 byte returned	Short
22h	10 0010	DCS Short READ Response, 2 bytes returned	Short

Data Types for Peripheral-sourced Packets

Acknowledge types		
Data type, hex	**Function description**	**Number of bytes**
02h	Get Acknowledge with Error report when Error occurs from processor transmission.	4 bytes
Note: When processor transmits complete Payload, following signal by BTA, peripheral must respond to processor. With error Acknowledge with error report, Without error Acknowledge.		

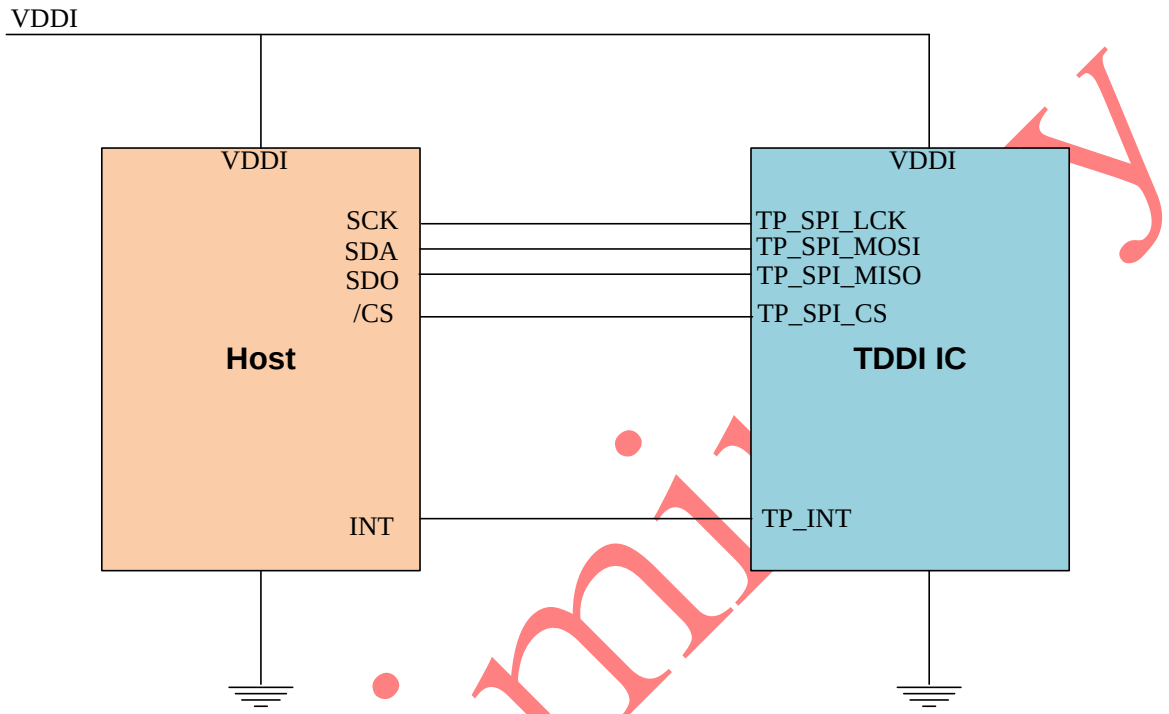
Generic Read types		
Data type, hex	**Function description**	**Number of bytes**
11h, 12h	This is the Generic Short Read Response, 1 or 2bytes, respectively.	4 bytes
1Ah	This is the long-packet response to Generic Long Read Request.	Up to 65541 bytes (DI + WC + ECC + DCS CMD + Payload DATA + PF)
Note: If the peripheral is Checksum capable, is shall return a calculated two-byte Checksum appended to the N-byte payload data. If the peripheral does not support Checksum, it shall return 0000h.If the DCS command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent after the Acknowledge with Error Report packet be sent.		

DCS Read types		
Data type, hex	**Function description**	**Number of bytes**
21h, 22h	This is the DCS Short Read Response, 1 or 2bytes, respectively..	4 bytes
1Ch	This is the long-packet response to DCS Long Read Request.	Up to 65541 bytes (DI + WC + ECC + DCS CMD + Payload DATA + PF)
Note: If the peripheral is Checksum capable, is shall return a calculated two-byte Checksum appended to the N-byte payload data. If the peripheral does not support Checksum, it shall return 0000h.If the DCS command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent after the Acknowledge with Error Report packet be sent.		

8.11 Touch Interface

8.11.1 SPI

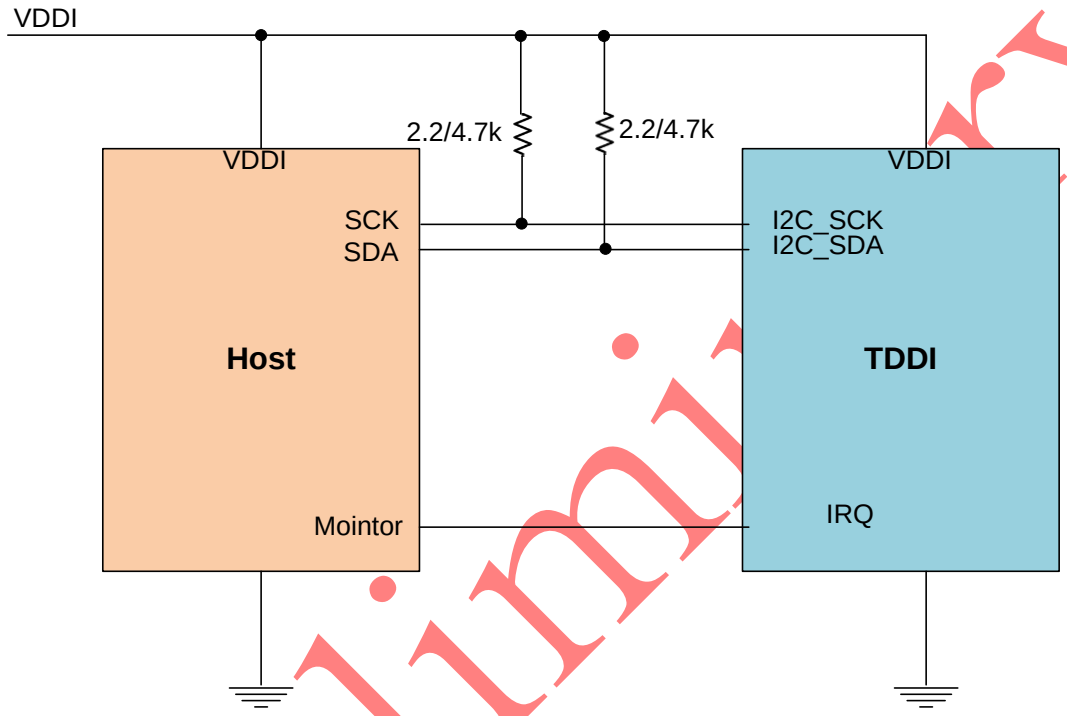
ST77922 operates as a SPI slave device and data length is 16-bit. SS, SCK, and MOSI are Schmitt trigger inputs. The data on MOSI is latched on rising edge of SCK and the data on MISO is outputted on falling edge of SCK.



8.11.2 I2C

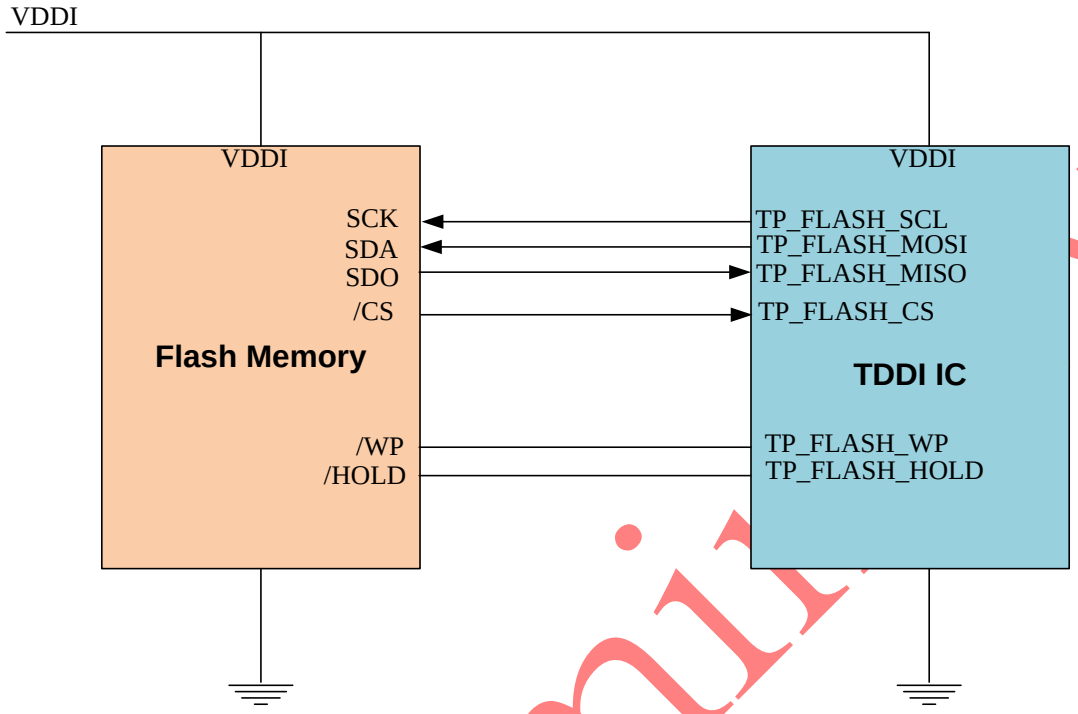
ST77922 protocol supports operating speeds of up to 400 kb/s with 7-bit addressing and 8-bit data bytes. The SCK, MOSI(SDA), and IRQ pins are typically used in an I2C interface.

The values of the pull-up resistors should be chosen to ensure that the rise times of the MOSI(SDA) and SCK signals are within the limits set by the I2C specification. These values depend on what other devices, if any, are on the I2Cbus. External pull-up resistors are of 2.2 kΩ or 4.7 kΩ.



8.11.3 Flash Memory

The master mode Flash serial peripheral Interface (SPI) communicate with Flash Memory and fetch the FW for Embedded MCU to achieve the touch function.



9 FUNCTION DESCRIPTION

9.1 Display Data RAM

9.1.1 Configuration

The display module has an integrated 200x400x24-bit graphic type static 1/2RAM. This bit memory allows storing on-chip a 400xRGBx400 image with an 24-bpp resolution (16.7M-color). There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

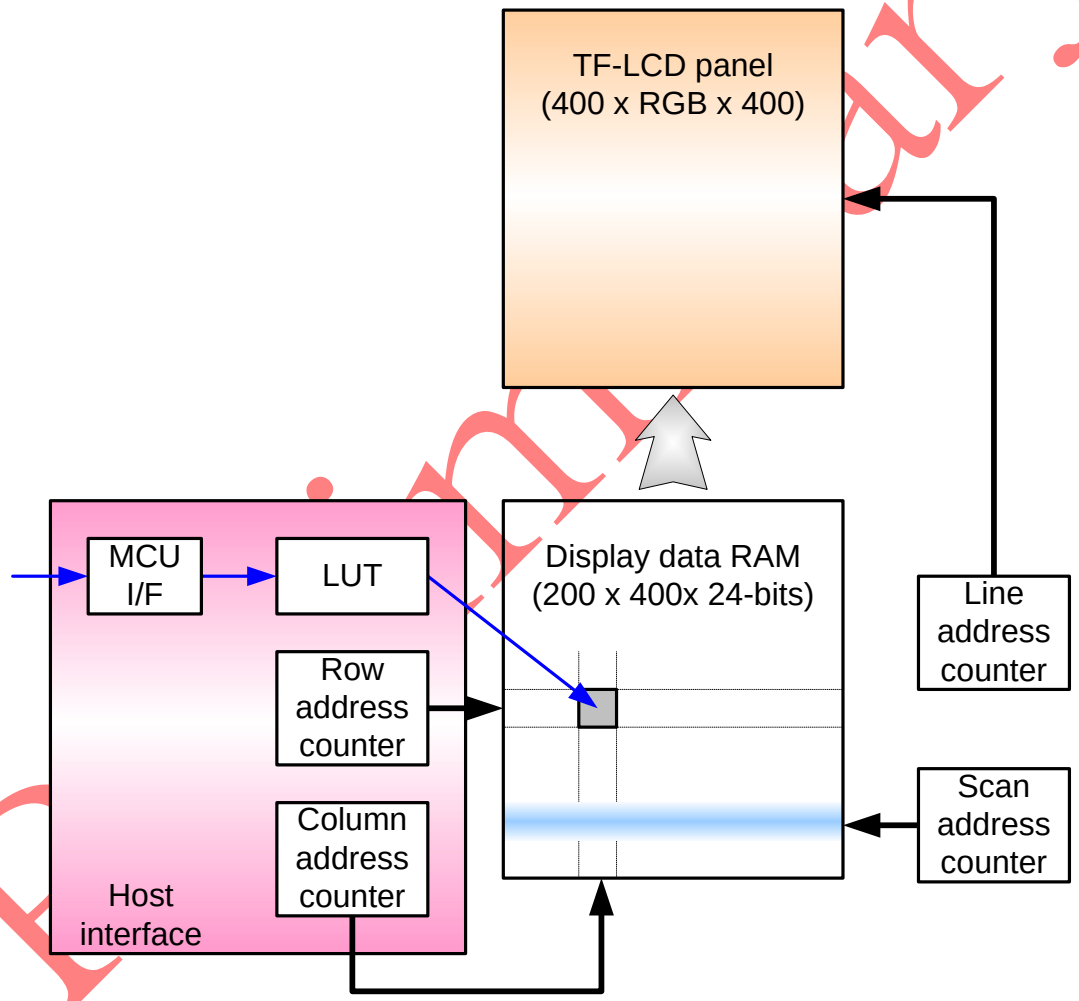
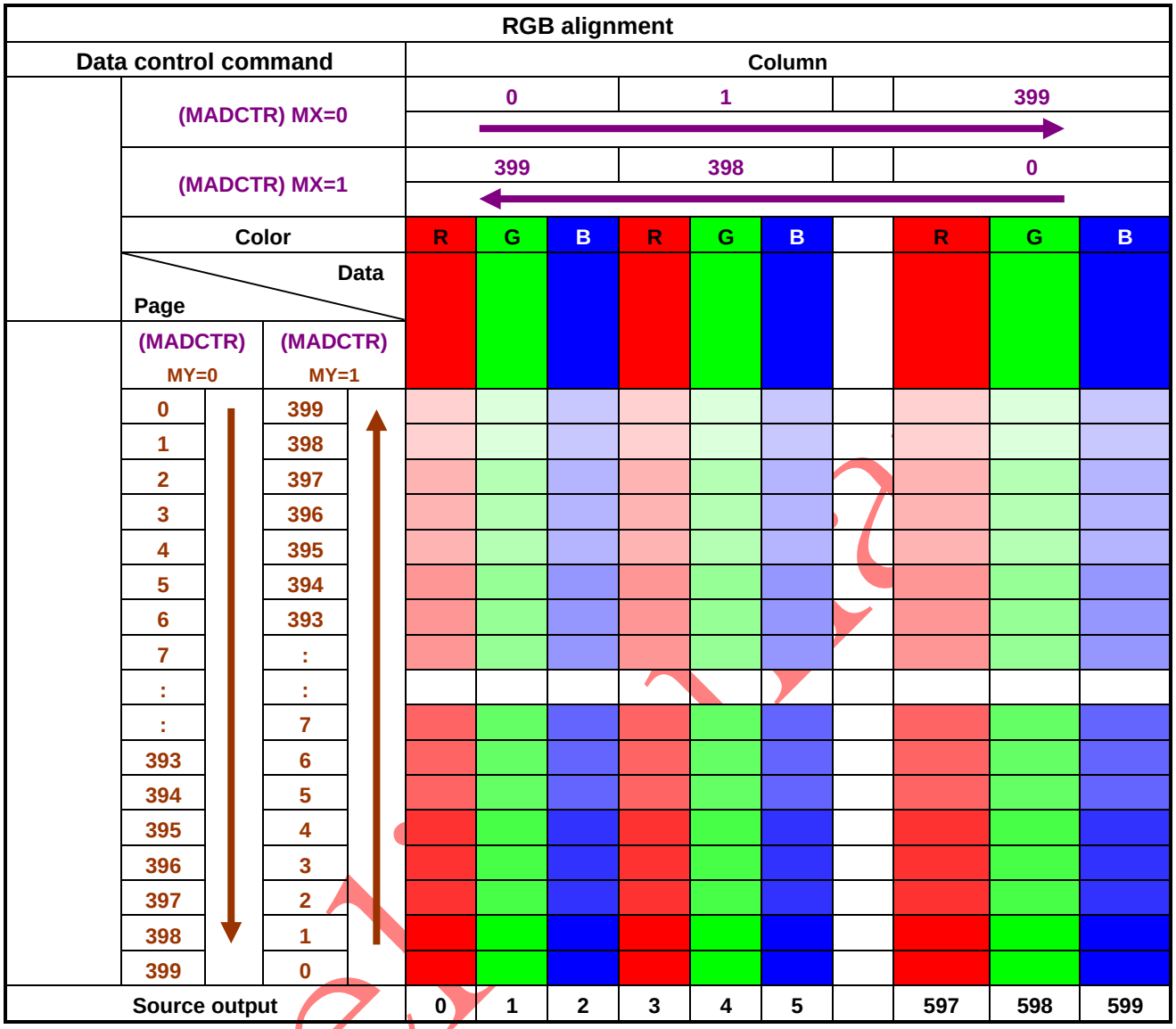


Figure 27 Display data RAM organization

9.1.2 Memory to display address mapping



9.2 Address Control

The address counter sets the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the “Write access” is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=399 (18Fh) and Y=0 to Y=399 (18Fh). Addresses outside these ranges are not allowed. Before writing to the RAM, a window must be defined that will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=399 (18Fh), YE=399 (18Fh).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands “CASET, RASET and MADCTL”, define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Section 8.12 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as below

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to “Start Column (XS)”	Return to “Start Row (YS)”
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than “End Column (XE)”	Return to “Start Column (XS)”	Increment by 1
The Column counter value is larger than “End Column (XE)” and the Row counter value is larger than “End Row (YE)”	Return to “Start Column (XS)”	Return to “Start Row (YS)”

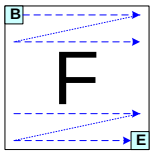
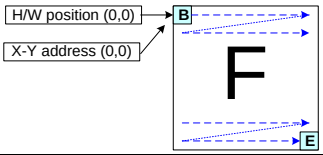
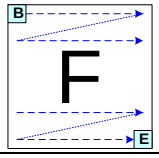
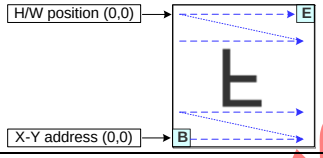
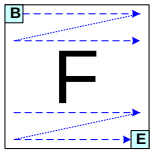
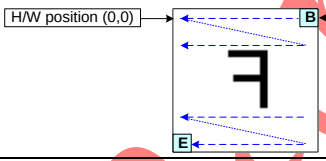
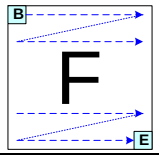
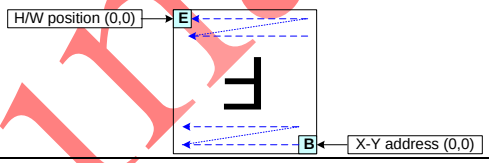
Display Data Direction	MADCTR Parameter		Image in the Host (MPU)	Image in the Driver (DDRAM)
	MX	MY		
Normal	0	0		
Y-Mirror	0	1		
X-Mirror	1	0		
X-Mirror Y-Mirror	1	1		

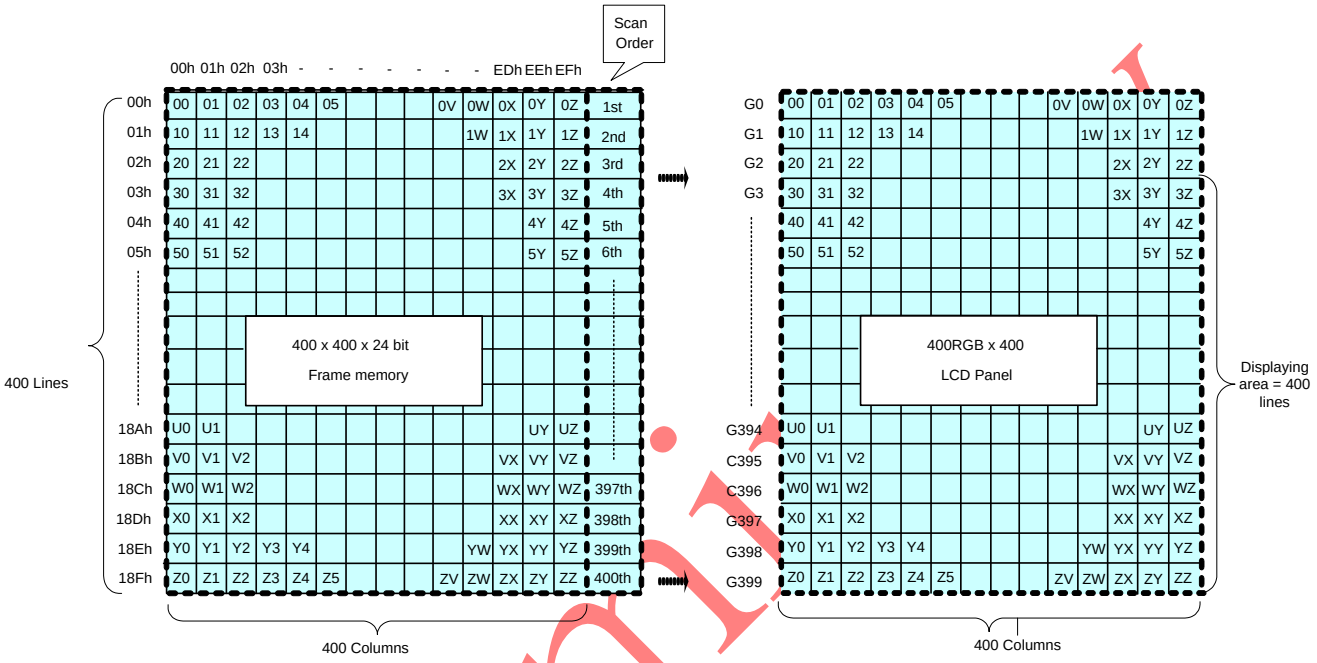
Figure 28 Display data RAM organization

9.3 Normal Display On or Partial Mode On, Vertical Scroll Off

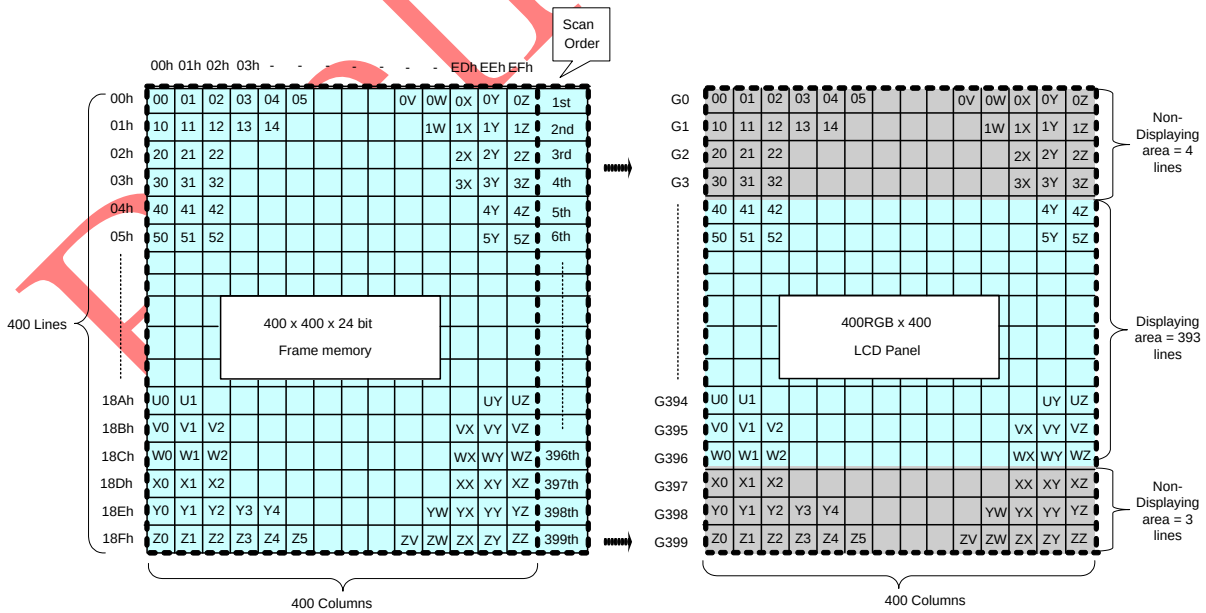
In this mode, contents of the frame memory within an area where column address is 00h to 83h and row address is 00h to 83h is displayed.

To display a dot on leftmost top corner, store the dot data at (column address, row address) = (0,0).

Example1) Normal Display On



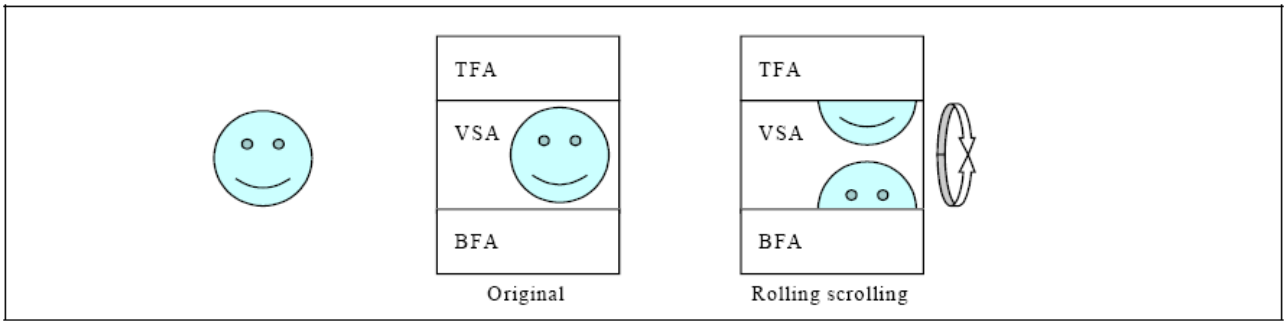
Example2) Partial Display On: PSL[15:0] = 0004h, PEL[15:0] = 013Ch, MADCTR (ML)=0



9.4 Vertical Scroll Mode

9.4.1 Rolling scroll

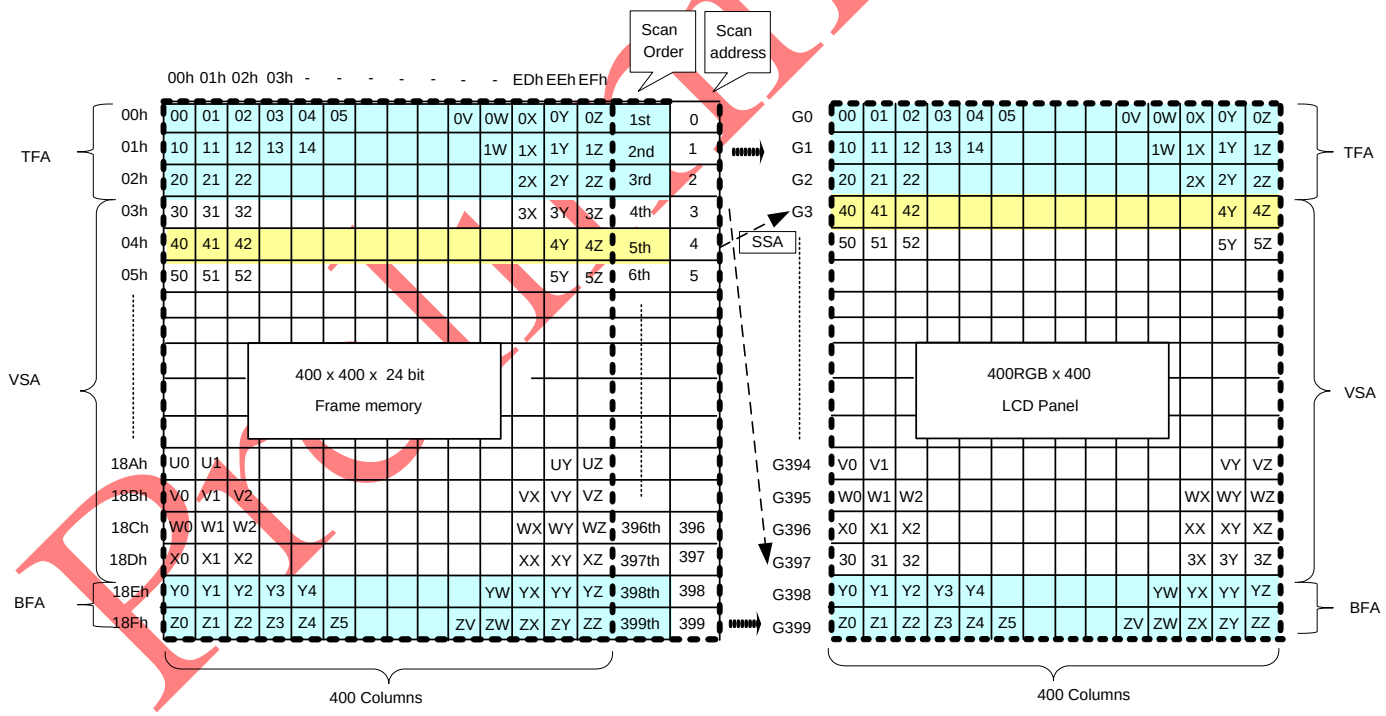
There is just one types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).



Rolling Scroll Definition

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) =400. In this case, ‘rolling’ scrolling is applied as shown below. All the memory contents will be used.

Example: Panel size=400 x 400, TFA =3, VSA=395, BFA=2, SSA=4, MADCTR ML=0: Rolling Scroll



9.4.2 Vertical Scroll Example

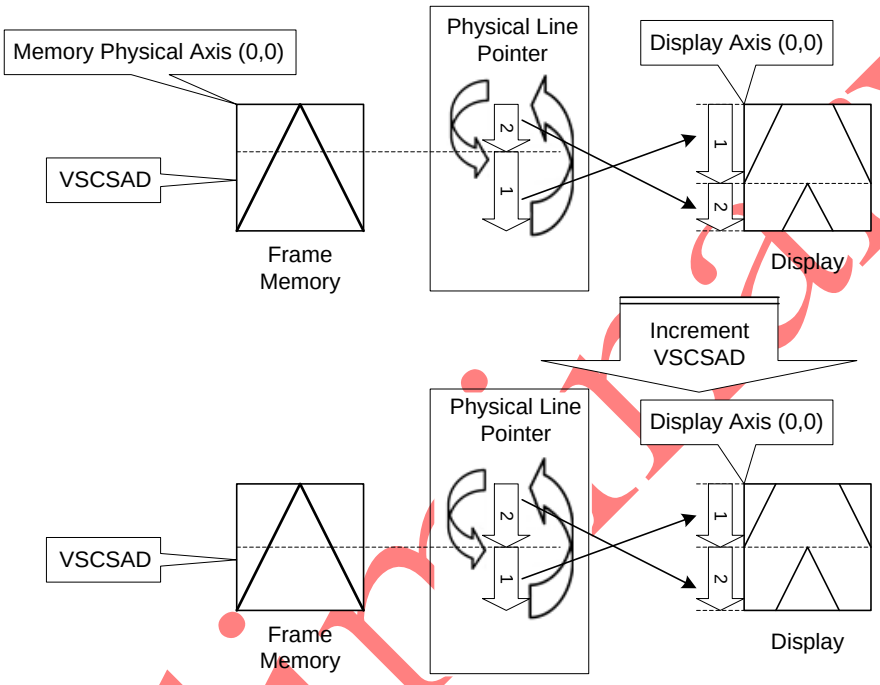
There are 2 types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

Case 1: TFA + VSA + BFA≠Panel total scan lines. In this case, scrolling is applied as shown below.

N/A. Do not set TFA + VSA + BFA≠Panel total scan lines. In that case, unexpected picture will be shown.

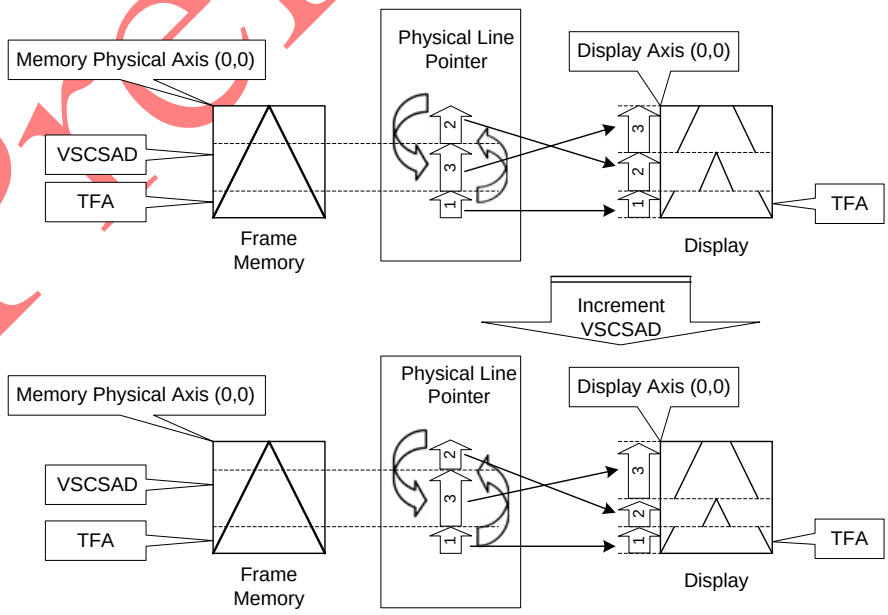
Case 2: TFA + VSA + BFA= Panel total scan lines

Example1) When MADCTR parameter ML=”0”, TFA=0, VSA=390, BFA=0 and VSCSAD=40.



Display of Vertical Scroll Example 1

Example2) When MADCTR parameter ML=”1”, TFA=60, VSA=340, BFA=0 and VSCSAD=160.



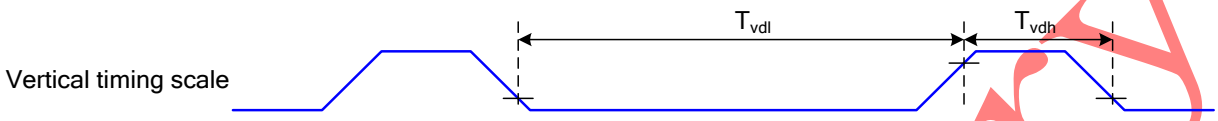
Display of Vertical Scroll Example 2

9.5 Tearing Effect

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

9.5.1 Tearing effect line modes

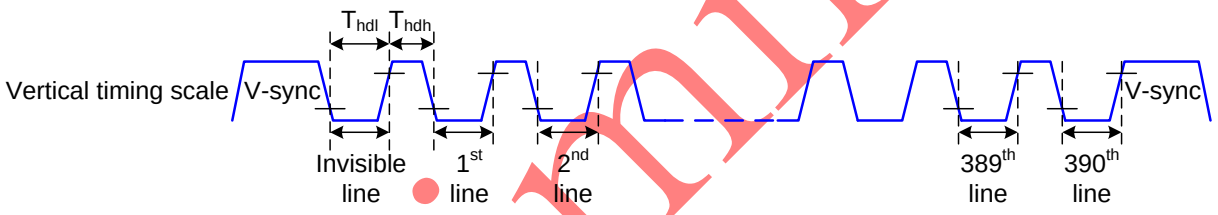
Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



tvdh= The LCD display is not updated from the Frame Memory

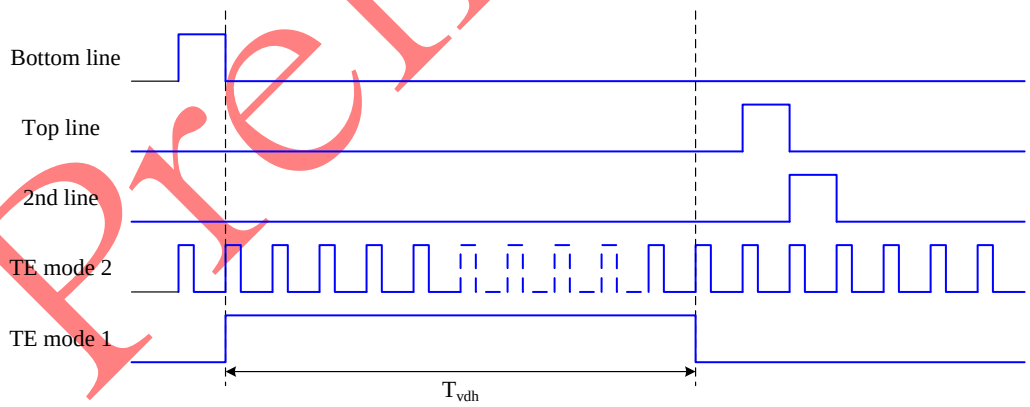
tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 390 H-sync pulses per field.



thdh= The LCD display is not updated from the Frame Memory

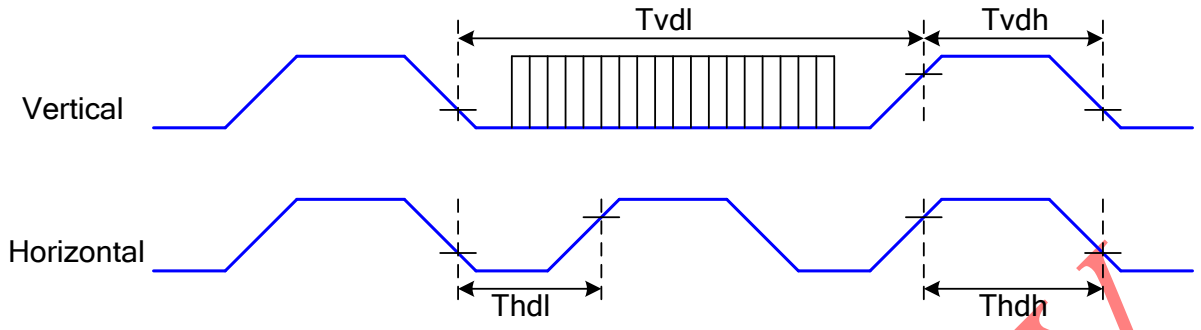
thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low.

9.5.2 Tearing effect line timings

The Tearing Effect signal is described below:



Symbol	Parameter	min	max	unit	description
tvdl	Vertical Timing Low Duration	13	-	ms	
tvdh	Vertical Timing High Duration	1000	-	µs	
thdl	Horizontal Timing Low Duration	16	-	µs	
thdh	Horizontal Timing Low Duration	-	500	µs	

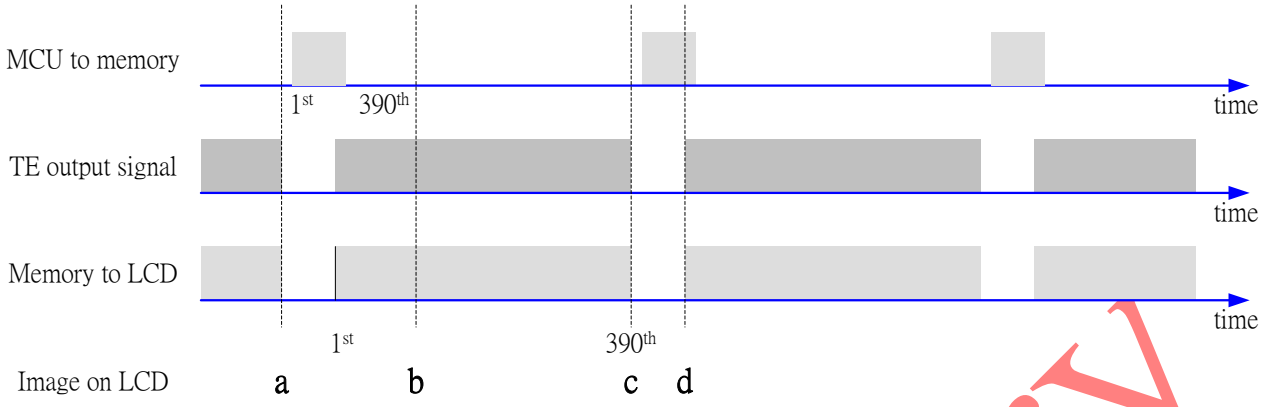
Table AC characteristics of Tearing Effect Signal Idle Mode Off (Frame Rate = 60 Hz, Ta=25°C)

Note: The timings in Table 15 apply when MADCTL ML=0 and ML=1

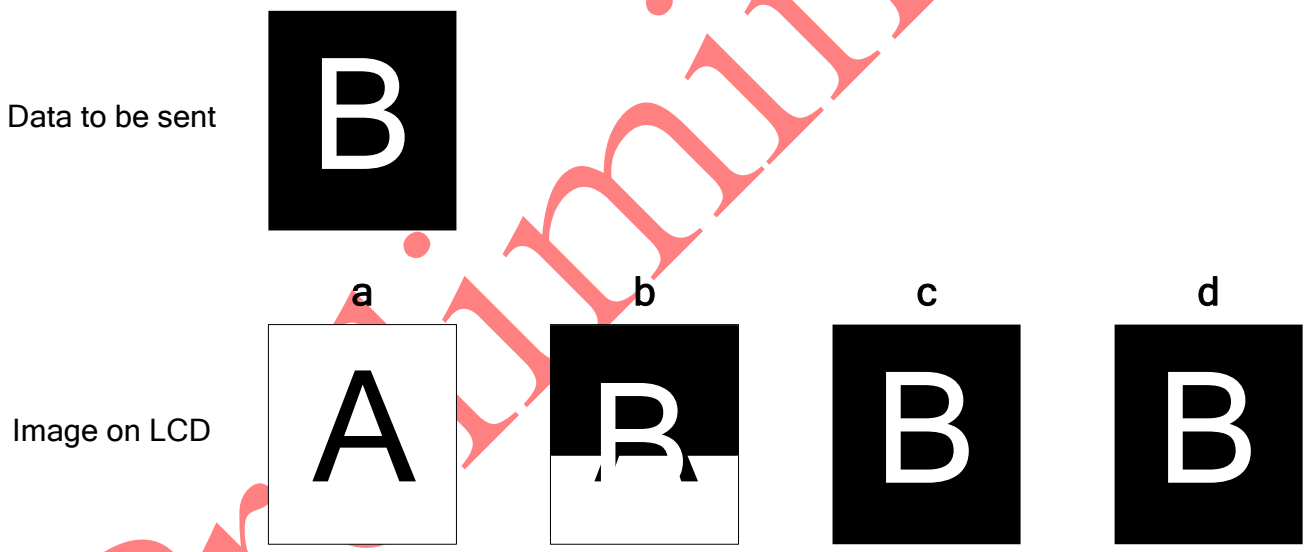
The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

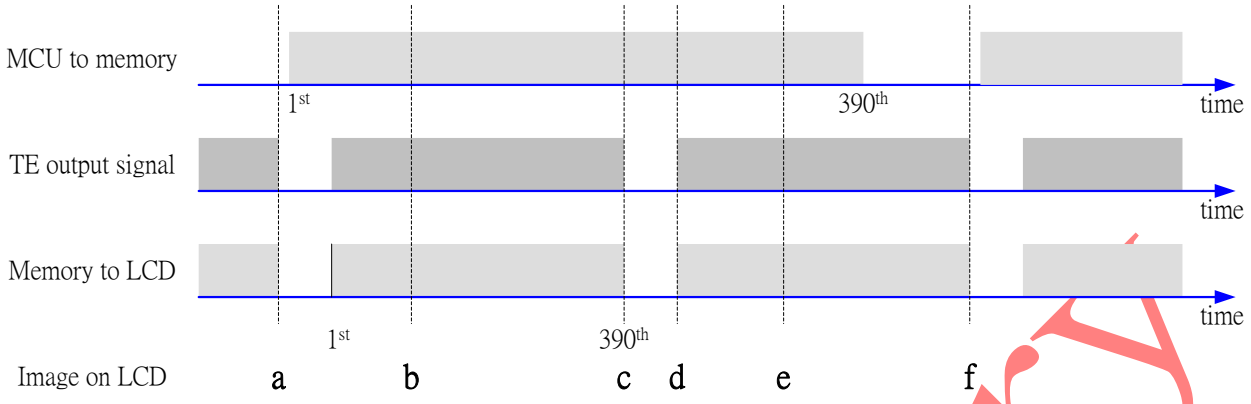
9.5.3 Example 1: MPU Write is faster than panel read



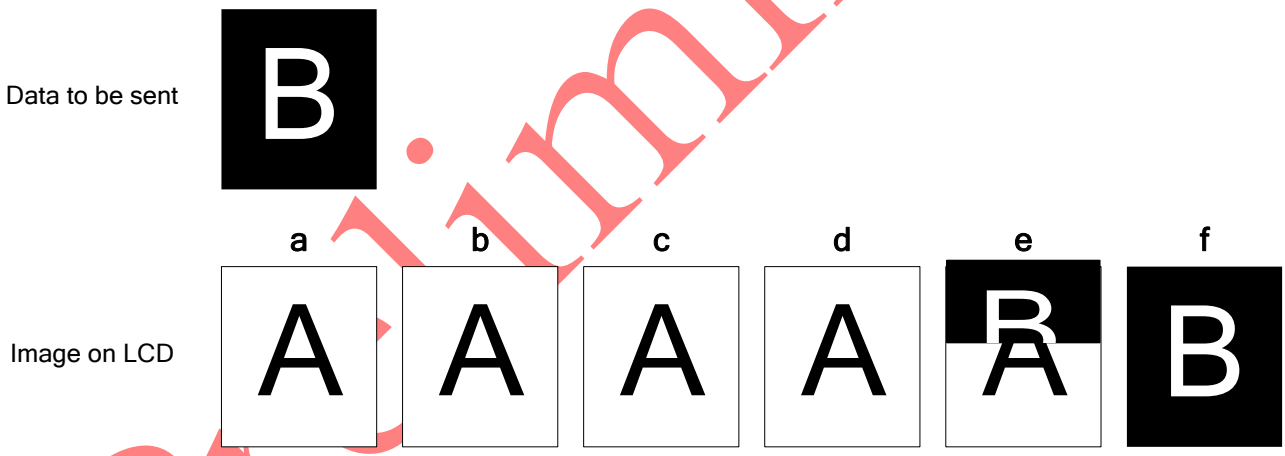
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



9.5.4 Example 2: MPU write is slower than panel read

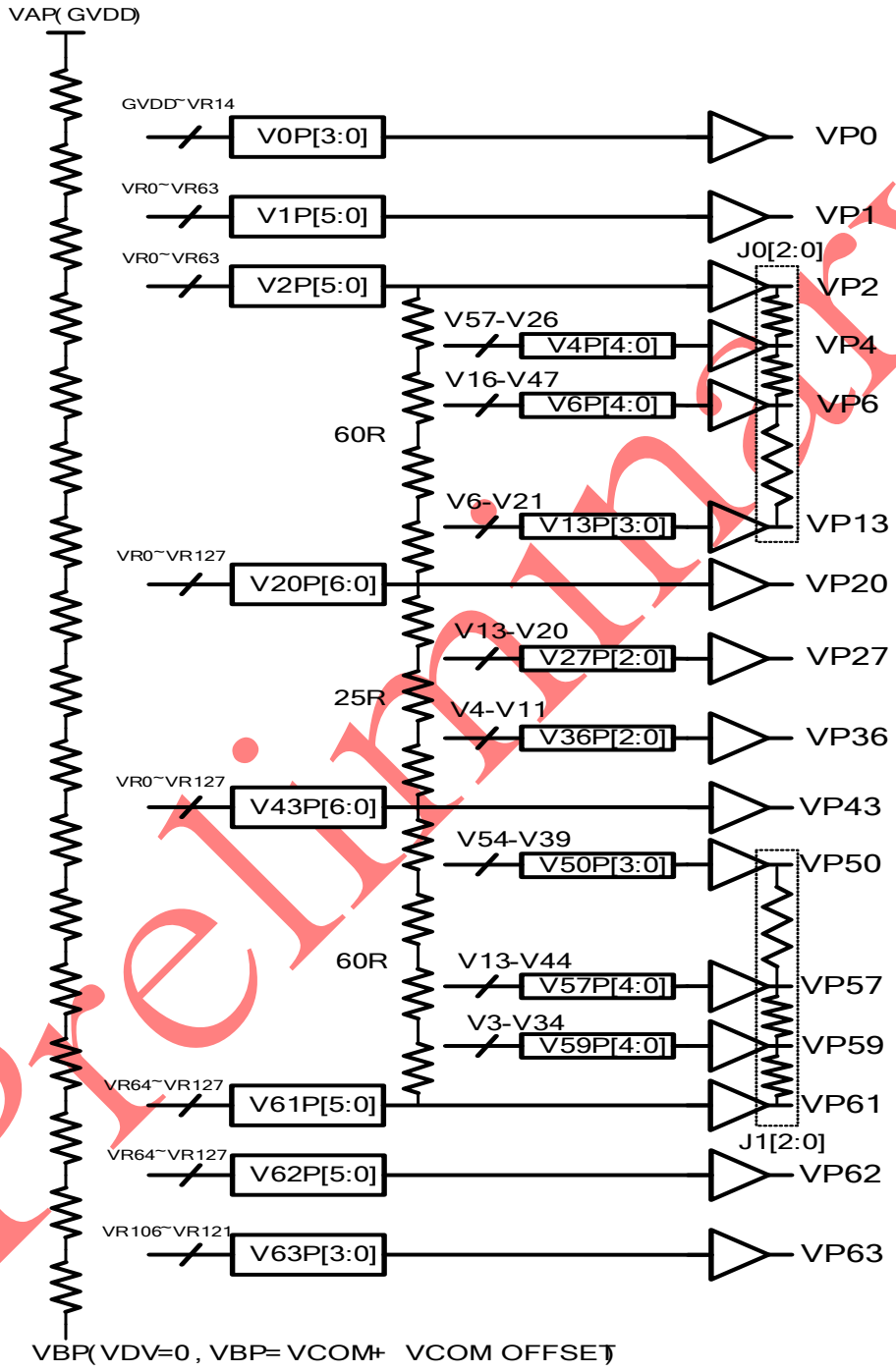


The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.

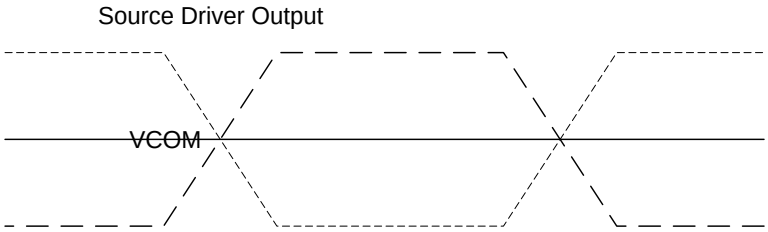


9.6 Gamma Correction

ST77922 incorporate the gamma correction function to display 16.7M colors for the LCD panel. The gamma correction is performed with 3 groups of registers, which are gradient adjustment, contrast adjustment and fine- adjustment registers for positive and negative polarities.



Gray scale Voltage Generation (Positive)



Relationship between Source Output and VCOM

Percentage adjustment:

VJ0P[2:0], VJ1P[2:0], VJ0N[2:0], VJ1N[2:0] these register are used to adjust the voltage level of interpolation point. The following table is the detail description.

VJ0P[2:0]/VJ0N[2:0]:

	00h	01h	02h	03h	04h	05h	06h	07h
VP3/VN3	50%,18	56%,20	50%,18	60%,22	42%,15	65%,23	45%,16	70%,25
VP5/VN5	50%,18	44%,16	50%,18	42%,15	65%,23	52%,19	40%,14	33%,12
VP7/VN7	86%,30	71%,25	80%,28	66%,23	88%,31	70%,25	76%,27	60%,21
VP8/VN8	71%,25	57%,20	63%,22	49%,17	61%,21	52%,18	58%,20	46%,16
VP9/VN9	57%,20	40%,14	49%,17	34%,12	60%,21	41%,15	47%,16	30%,11
VP10/VN10	43%,15	29%,10	34%,12	23%,8	46%,16	25%,9	36%,13	20%,7
VP11/VN11	29%,10	17%,6	20%,7	14%,5	32%,11	26%,9	23%,8	12%,4
VP12/VN12	14%,5	6%,2	9%,3	6%,2	20%,7	11%,4	17%,6	3%,1

VJ1P[2:0]/VJ1N[2:0]:

	00h	01h	02h	03h	04h	05h	06h	07h
VP51/VN51	86%,30	86%,30	86%,30	89%,31	77%,27	92%,32	83%,29	95%,33
VP52/VN52	71%,25	71%,25	77%,27	80%,28	63%,22	69%,24	75%,26	83%,29
VP53/VN53	57%,20	60%,21	63%,22	69%,24	48%,17	54%,19	66%,23	72%,25
VP54/VN54	43%,15	46%,16	46%,16	51%,18	35%,12	41%,14	55%,19	60%,21
VP55/VN55	29%,10	34%,12	31%,11	37%,13	23%,8	40%,14	26%,9	43%,15
VP56/VN56	14%,5	17%,6	14%,5	20%,7	9%,3	23%,8	11%,4	26%,9
VP58/VN58	50%,18	56%,20	47%,17	47%,17	53%,19	59%,21	45%,16	42%,15
VP60/VN60	50%,18	50%,18	50%,18	53%,19	42%,15	45%,16	55%,20	60%,21

voltage level percentage adjustment description

Source voltage of positive gamma level

Gamma level	Related Register	Formula
VP0	V0P[3:0]	(VAP-VBP)*(129R-V0P[3:0]R)/129R+VBP
VP1	V1P[5:0]	(VAP-VBP)*(128R-V1P[5:0]R)/129R+VBP
VP2	V2P[5:0]	(VAP-VBP)*(128R-V2P[5:0]R)/129R+VBP
VP3	VJ0P[2:0]	(VP2-VP4)* VJ0P[2:0]+VP4
VP4	V4P[4:0]	(VP2-VP20)*(57R-V4P[4:0])/60R+VP20
VP5	VJ0P[2:0]	(VP4-VP6)* VJ0P[2:0]+VP6
VP6	V6P[4:0]	(VP2-VP20)*(47R-V6P[4:0])/60R+VP20
VP7	VJ0P[2:0]	(VP6-VP13)* VJ0P[2:0]+VP13
VP8	VJ0P[2:0]	(VP6-VP13)* VJ0P[2:0]+VP13
VP9	VJ0P[2:0]	(VP6-VP13)* VJ0P[2:0]+VP13
VP10	VJ0P[2:0]	(VP6-VP13)* VJ0P[2:0]+VP13
VP11	VJ0P[2:0]	(VP6-VP13)* VJ0P[2:0]+VP13
VP12	VJ0P[2:0]	(VP6-VP13)* VJ0P[2:0]+VP13
VP13	V13P[3:0]	(VP2-VP20)*(21R-V13P[3:0])/60R+VP20
VP14	--	(VP13-VP20)/(20-13)*(20-14)+VP20
VP15	--	(VP13-VP20)/(20-13)*(20-15)+VP20
VP16	--	(VP13-VP20)/(20-13)*(20-16)+VP20
VP17	--	(VP13-VP20)/(20-13)*(20-17)+VP20
VP18	--	(VP13-VP20)/(20-13)*(20-18)+VP20
VP19	--	(VP13-VP20)/(20-13)*(20-19)+VP20
VP20	V20P[6:0]	(VAP-VBP)*(128R-V20P[6:0]R)/129R+VBP
VP21	--	(VP20-VP27)/(27-20)*(27-21)+VP27
VP22	--	(VP20-VP27)/(27-20)*(27-22)+VP27
VP23	--	(VP20-VP27)/(27-20)*(27-23)+VP27
VP24	--	(VP20-VP27)/(27-20)*(27-24)+VP27
VP25	--	(VP20-VP27)/(27-20)*(27-25)+VP27
VP26	--	(VP20-VP27)/(27-20)*(27-26)+VP27
VP27	V27P[2:0]	(VP20-VP43)*(20R-V27P[2:0])/25R+VP43
VP28	--	(VP27-VP36)/(36-27)*(36-28)+VP36
VP29	--	(VP27-VP36)/(36-27)*(36-29)+VP36
VP30	--	(VP27-VP36)/(36-27)*(36-30)+VP36
VP31	--	(VP27-VP36)/(36-27)*(36-31)+VP36
VP32	--	(VP27-VP36)/(36-27)*(36-32)+VP36
VP33	--	(VP27-VP36)/(36-27)*(36-33)+VP36
VP34	--	(VP27-VP36)/(36-27)*(36-34)+VP36
VP35	--	(VP27-VP36)/(36-27)*(36-35)+VP36
VP36	V36P[2:0]	(VP20-VP43)*(11R-V36P[2:0])/25R+VP43
VP37	--	(VP36-VP43)/(43-36)*(43-37)+VP43
VP38	--	(VP36-VP43)/(43-36)*(43-38)+VP43
VP39	--	(VP36-VP43)/(43-36)*(43-39)+VP43
VP40	--	(VP36-VP43)/(43-36)*(43-40)+VP43
VP41	--	(VP36-VP43)/(43-36)*(43-41)+VP43
VP42	--	(VP36-VP43)/(43-36)*(43-42)+VP43
VP43	V43P[6:0]	(VAP-VBP)*(128R-V43P[6:0]R)/129R+VBP
VP44	--	(VP43-VP50)/(50-43)*(50-44)+VP50
VP45	--	(VP43-VP50)/(50-43)*(50-45)+VP50
VP46	--	(VP43-VP50)/(50-43)*(50-46)+VP50
VP47	--	(VP43-VP50)/(50-43)*(50-47)+VP50
VP48	--	(VP43-VP50)/(50-43)*(50-48)+VP50
VP49	--	(VP43-VP50)/(50-43)*(50-49)+VP50
VP50	V50P[3:0]	(VP43-VP61)*(54R-V50P[3:0])/60R+VP61
VP51	VJ1P[2:0]	(V5P0-VP57)*VJ1P[2:0]+VP57
VP52	VJ1P[2:0]	(VP50-VP57)* VJ1P[2:0]+VP57

VP53	VJ1P[2:0]	(VP50-VP57)* VJ1P[2:0]+VP57
VP54	VJ1P[2:0]	(VP50-VP57)* VJ1P[2:0]+VP57
VP55	VJ1P[2:0]	(VP50-VP57)* VJ1P[2:0]+VP57
VP56	VJ1P[2:0]	(VP50-VP57)* VJ1P[2:0]+VP57
VP57	V57P[4:0]	(VP43-VP61)*(44R-V57P[4:0])/60R+VP61
VP58	VJ1P[2:0]	(VP57-VP59)* VJ1P[2:0]+VP59
VP59	V59P[4:0]	(VP43-VP61)*(34R-V59P[4:0])/60R+VP61
VP60	VJ1P[2:0]	(VP59-VP61)* VJ1P[2:0]+VP61
VP61	V61P[5:0]	(VAP-VBP)*(64R-V61P[5:0]R)/129R+VBP
VP62	V62P[5:0]	(VAP-VBP)*(64R-V62P[5:0]R)/129R+VBP
VP63	V63P[3:0]	(VAP-VBP)*(23R-V63P[3:0]R)/129R+VBP

Source voltage of negative gamma level

Gamma level	Related Register	Formula
VN0	V0N[3:0]	VBN-(VBN-VAN)*(129R-V0N[3:0]R)/129R
VN1	V1N[5:0]	VBN-(VBN-VAN)*(128R-V1N[5:0]R)/129R
VN2	V2N[5:0]	VBN-(VBN-VAN)*(128R-V2N[5:0]R)/129R
VN3	VJ0N[2:0]	(VN2-VN4)*VJ0N[2:0]+VN4
VN4	V4N[4:0]	(VN2-VN20)*(57R-V4N[4:0])/60R+VN20
VN5	VJ0N[2:0]	(VN4-VN6)* VJ0N[2:0]+VN6
VN6	V6N[4:0]	(VN2-VN20)*(47R-V6N[4:0])/60R+VN20
VN7	VJ0N[2:0]	(VN6-VN13)* VJ0N[2:0]+VN13
VN8	VJ0N[2:0]	(VN6-VN13)* VJ0N[2:0]+VN13
VN9	VJ0N[2:0]	(VN6-VN13)* VJ0N[2:0]+VN13
VN10	VJ0N[2:0]	(VN6-VN13)* VJ0N[2:0]+VN13
VN11	VJ0N[2:0]	(VN6-VN13)* VJ0N[2:0]+VN13
VN12	VJ0N[2:0]	(VN6-VN13)* VJ0N[2:0]+VN13
VN13	V13N[3:0]	(VN2-VN20)*(21R-V13N[3:0])/60R+VN20
VN14	--	(VN13-VN20)/(20-13)*(20-14)+VN20
VN15	--	(VN13-VN20)/(20-13)*(20-15)+VN20
VN16	--	(VN13-VN20)/(20-13)*(20-16)+VN20
VN17	--	(VN13-VN20)/(20-13)*(20-17)+VN20
VN18	--	(VN13-VN20)/(20-13)*(20-18)+VN20
VN19	--	(VN13-VN20)/(20-13)*(20-19)+VN20
VN20	V20N[6:0]	VBN-(VBN-VAN)*(128R-V20N[6:0]R)/129R
VN21	--	(VN20-VN27)/(27-20)*(27-21)+VN27
VN22	--	(VN20-VN27)/(27-20)*(27-22)+VN27
VN23	--	(VN20-VN27)/(27-20)*(27-23)+VN27
VN24	--	(VN20-VN27)/(27-20)*(27-24)+VN27
VN25	--	(VN20-VN27)/(27-20)*(27-25)+VN27
VN26	--	(VN20-VN27)/(27-20)*(27-26)+VN27
VN27	V27N[2:0]	(VN20-VN43)*(20R-V27N[2:0])/25R+VN43
VN28	--	(VN27-VN36)/(36-27)*(36-28)+VN36
VN29	--	(VN27-VN36)/(36-27)*(36-29)+VN36
VN30	--	(VN27-VN36)/(36-27)*(36-30)+VN36
VN31	--	(VN27-VN36)/(36-27)*(36-31)+VN36
VN32	--	(VN27-VN36)/(36-27)*(36-32)+VN36
VN33	--	(VN27-VN36)/(36-27)*(36-33)+VN36
VN34	--	(VN27-VN36)/(36-27)*(36-34)+VN36
VN35	--	(VN27-VN36)/(36-27)*(36-35)+VN36
VN36	V36N[2:0]	(VN20-VN43)*(11R-V36N[2:0])/25R+VN43
VN37	--	(VN36-VN43)/(43-36)*(43-37)+VN43
VN38	--	(VN36-VN43)/(43-36)*(43-38)+VN43
VN39	--	(VN36-VN43)/(43-36)*(43-39)+VN43

VN40	--	(VN36-VN43)/(43-36)*(43-40)+VN43
VN41	--	(VN36-VN43)/(43-36)*(43-41)+VN43
VN42	--	(VN36-VN43)/(43-36)*(43-42)+VN43
VN43	V43N[6:0]	VBN-(VBN-VAN)*(128R-V43N[6:0]R)/129R
VN44	--	(VN43-VN50)/(50-43)*(50-44)+VN50
VN45	--	(VN43-VN50)/(50-43)*(50-45)+VN50
VN46	--	(VN43-VN50)/(50-43)*(50-46)+VN50
VN47	--	(VN43-VN50)/(50-43)*(50-47)+VN50
VN48	--	(VN43-VN50)/(50-43)*(50-48)+VN50
VN49	--	(VN43-VN50)/(50-43)*(50-49)+VN50
VN50	V50N[3:0]	(VN43-VN61)*(54R-V50N[3:0])/60R+VN61
VN51	VJ1N[2:0]	(V5N0-VN57)*VJ1N[2:0]+VN57
VN52	VJ1N[2:0]	(VN50-VN57)* VJ1N[2:0]+VN57
VN53	VJ1N[2:0]	(VN50-VN57)* VJ1N[2:0]+VN57
VN54	VJ1N[2:0]	(VN50-VN57)* VJ1N[2:0]+VN57
VN55	VJ1N[2:0]	(VN50-VN57)* VJ1N[2:0]+VN57
VN56	VJ1N[2:0]	(VN50-VN57)* VJ1N[2:0]+VN57
VN57	V57N[4:0]	(VN43-VN61)*(44R-V57N[4:0])/60R+VN61
VN58	VJ1N[2:0]	(VN57-VN59)* VJ1N[2:0]+VN59
VN59	V59N[4:0]	(VN43-VN61)*(34R-V59N[4:0])/60R+VN61
VN60	VJ1N[2:0]	(VN59-VN61)* VJ1N[2:0]+VN61
VN61	V61N[5:0]	VBN-(VBN-VAN)*(64R-V61N[5:0]R)/129R
VN62	V62N[5:0]	VBN-(VBN-VAN)*(64R-V62N[5:0]R)/129R
VN63	V63N[3:0]	VBN-(VBN-VAN)*(23R-V63N[3:0]R)/129R

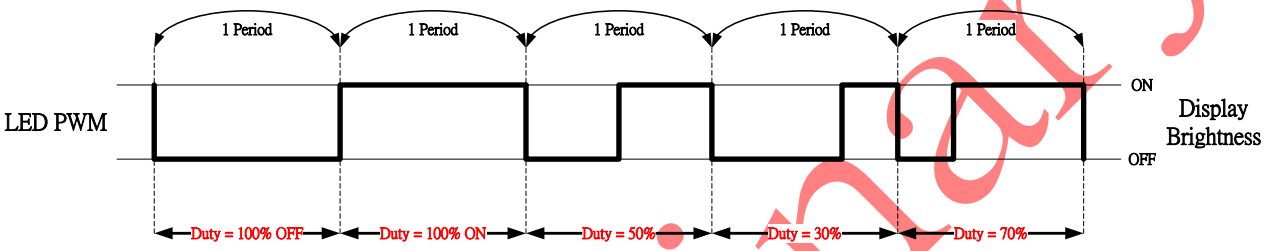
9.7 Brightness Control Block

There is an external output signal from brightness block, LEDPWM to control the LED driver IC in order to control display brightness.

There are register bits, R51h, DBV[7:0] for display brightness of manual brightness setting. The LEDPWM duty is calculated as DBV[7:0] / 255 x Period (affected by OSC frequency).

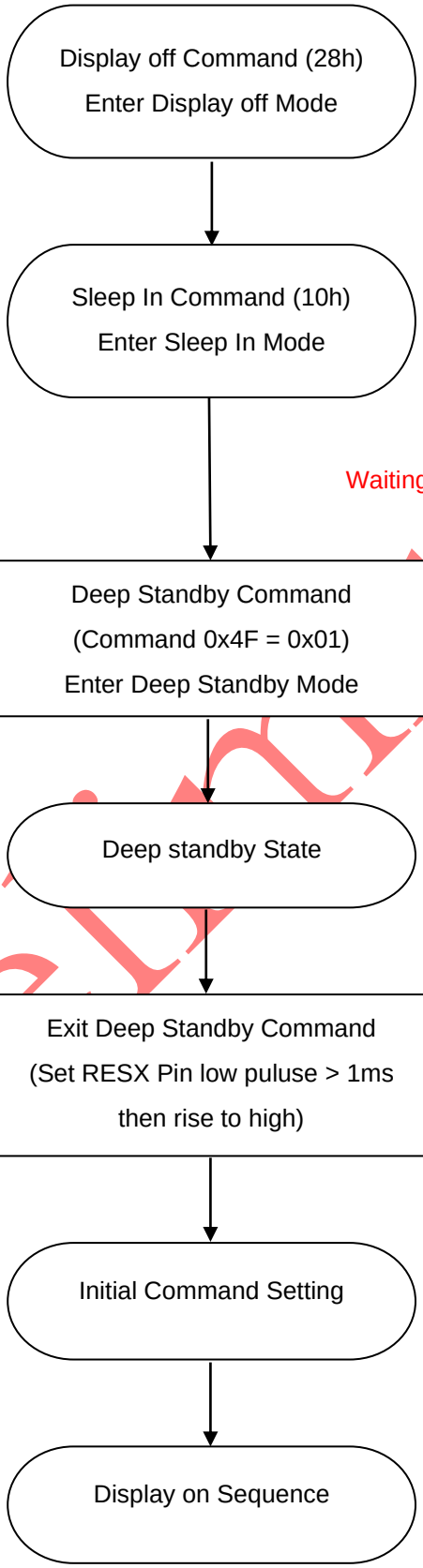
For example: LEDPWM period = 3 ms, and DBV[7:0] = ‘200’. Then LEDPWM duty = 200 / 255 = 78.1%.

Correspond to the LEDPWM period = 3 ms, the high-level of LEDPWM (high effective) = 2.344 ms, and the low-level of LEDPWM = 0.656 m



LEDPWM Output Duty

9.8 Deep Standby mode



10 POWER DEFINITION

10.1 Power Level

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 262,144 colors.

2. Normal Mode Off (full display), Idle Mode Off, Sleep Out.

In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display area is used but with 8 colors.

4. Normal Mode Off (full display), Idle Mode On, Sleep Out.

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode

In this mode, the DC:DC converter, internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.

6. Power Off Mode

In this mode, both VDD and VDDI are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

10.2 Power ON/OFF Sequence

VDDI and VDD can be applied in any order.

VDD and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

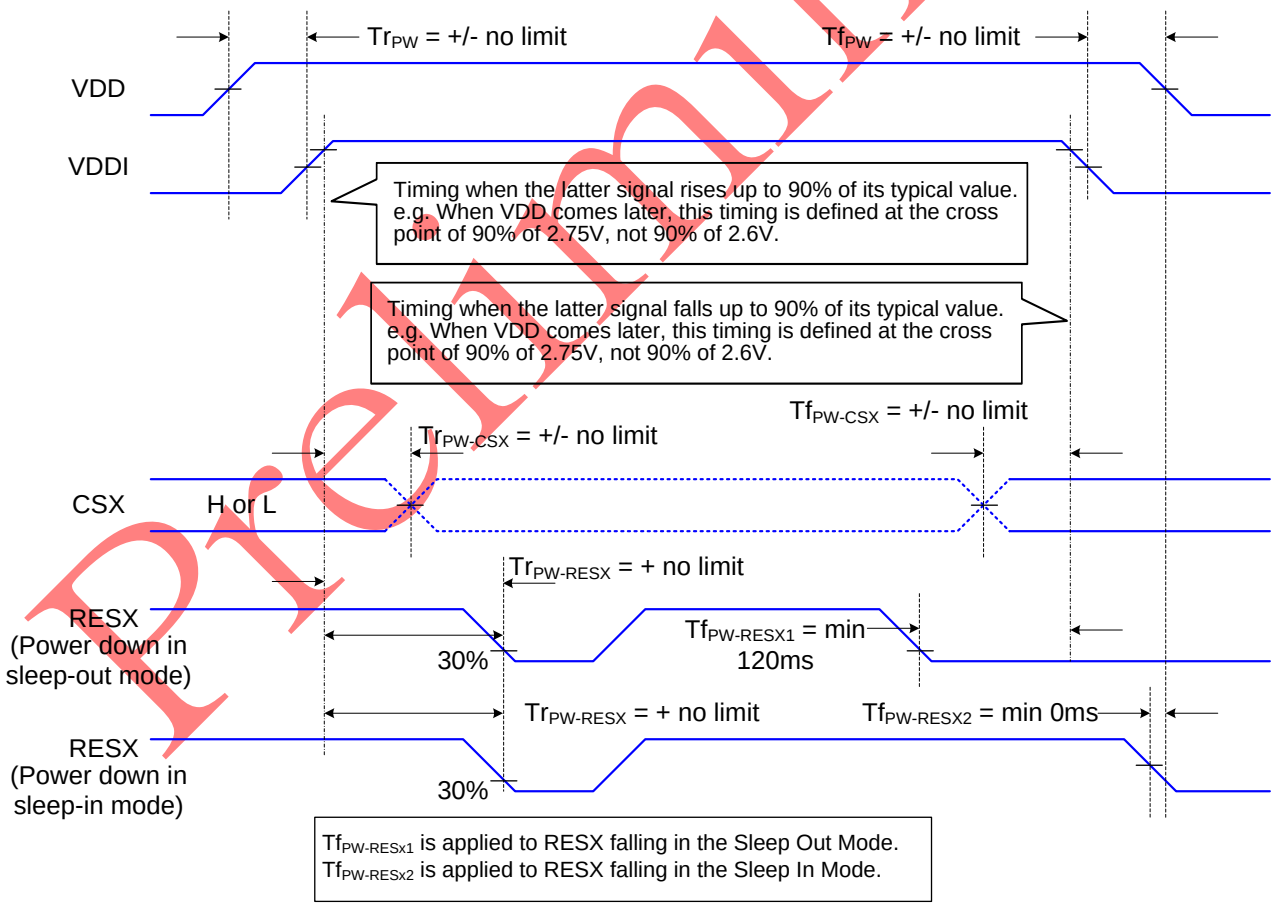
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



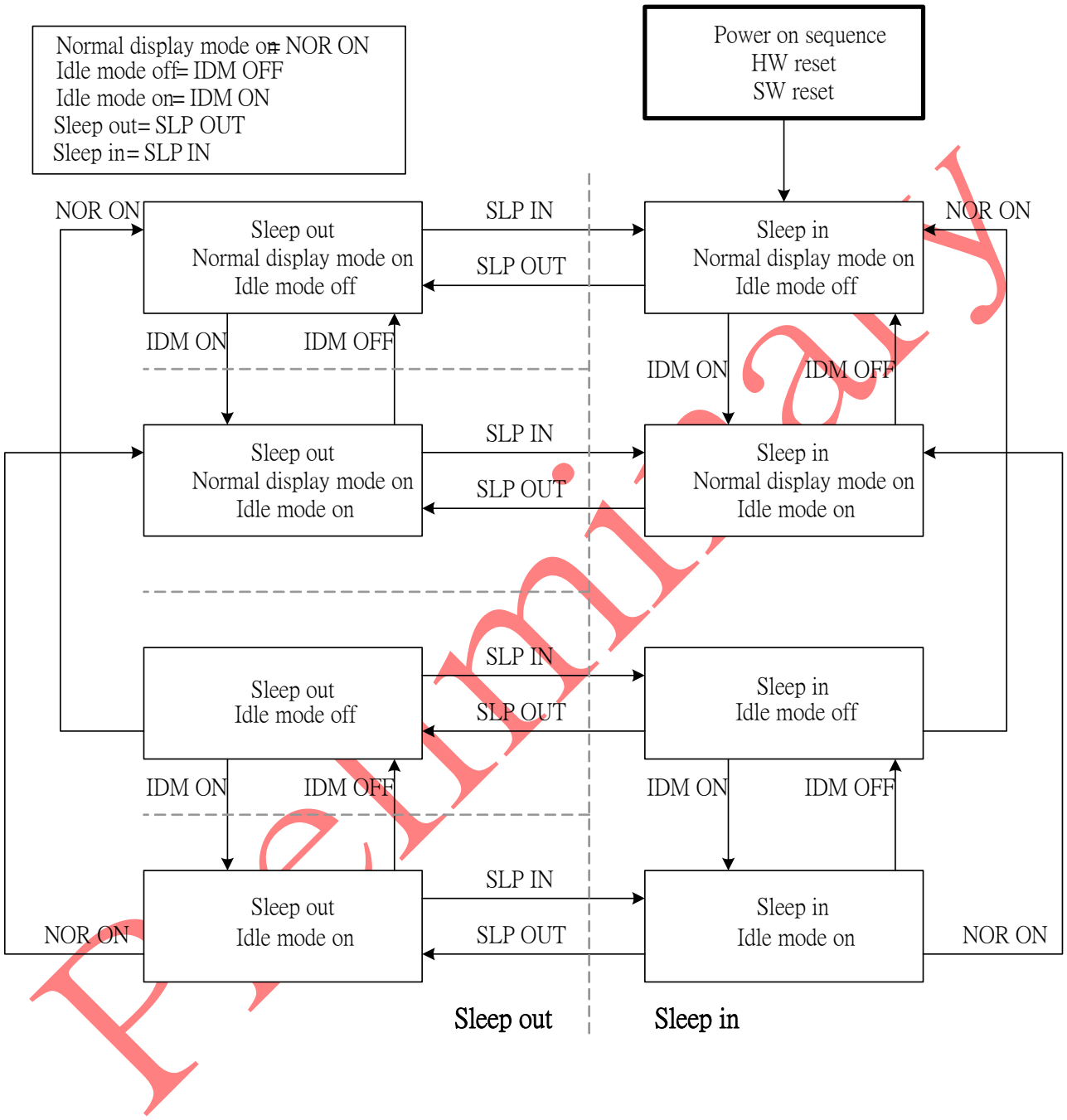
10.3 Uncontrolled Power OFF

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

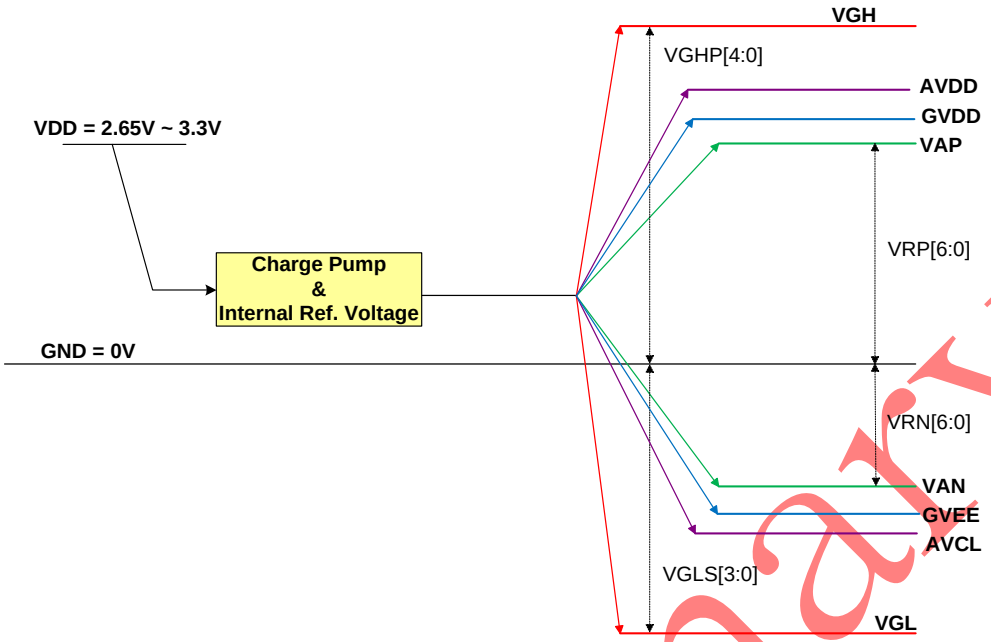
If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display

(blank display) and remains blank until “Power On Sequence” powers it up.

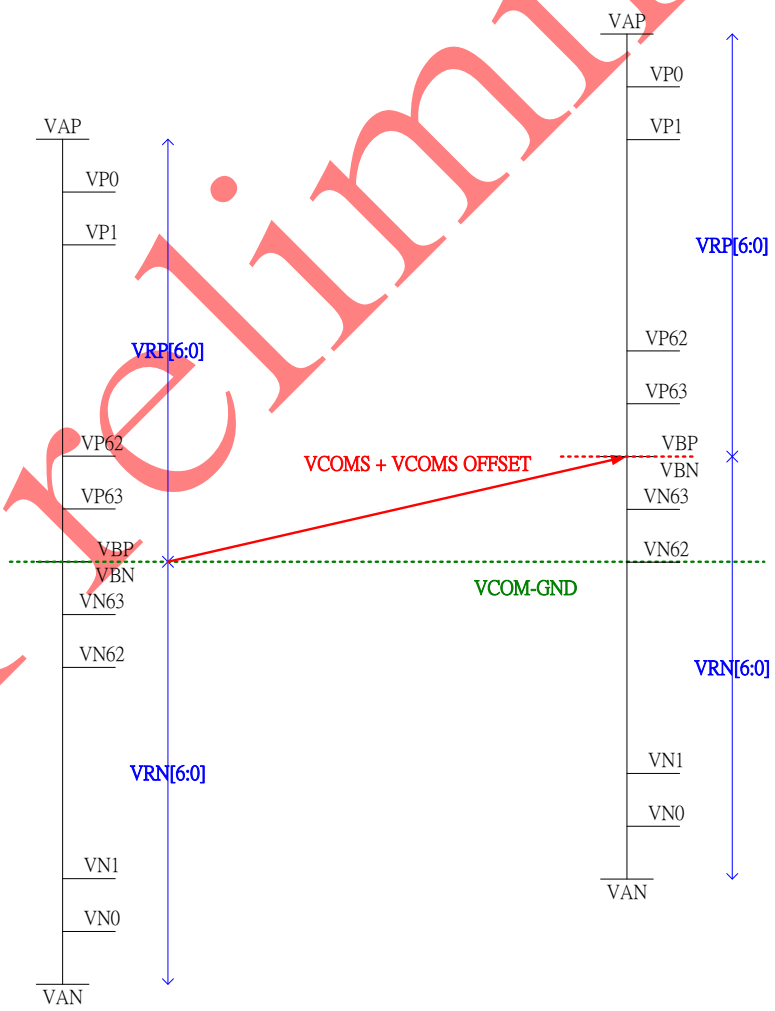
10.4 Power Flow Chart



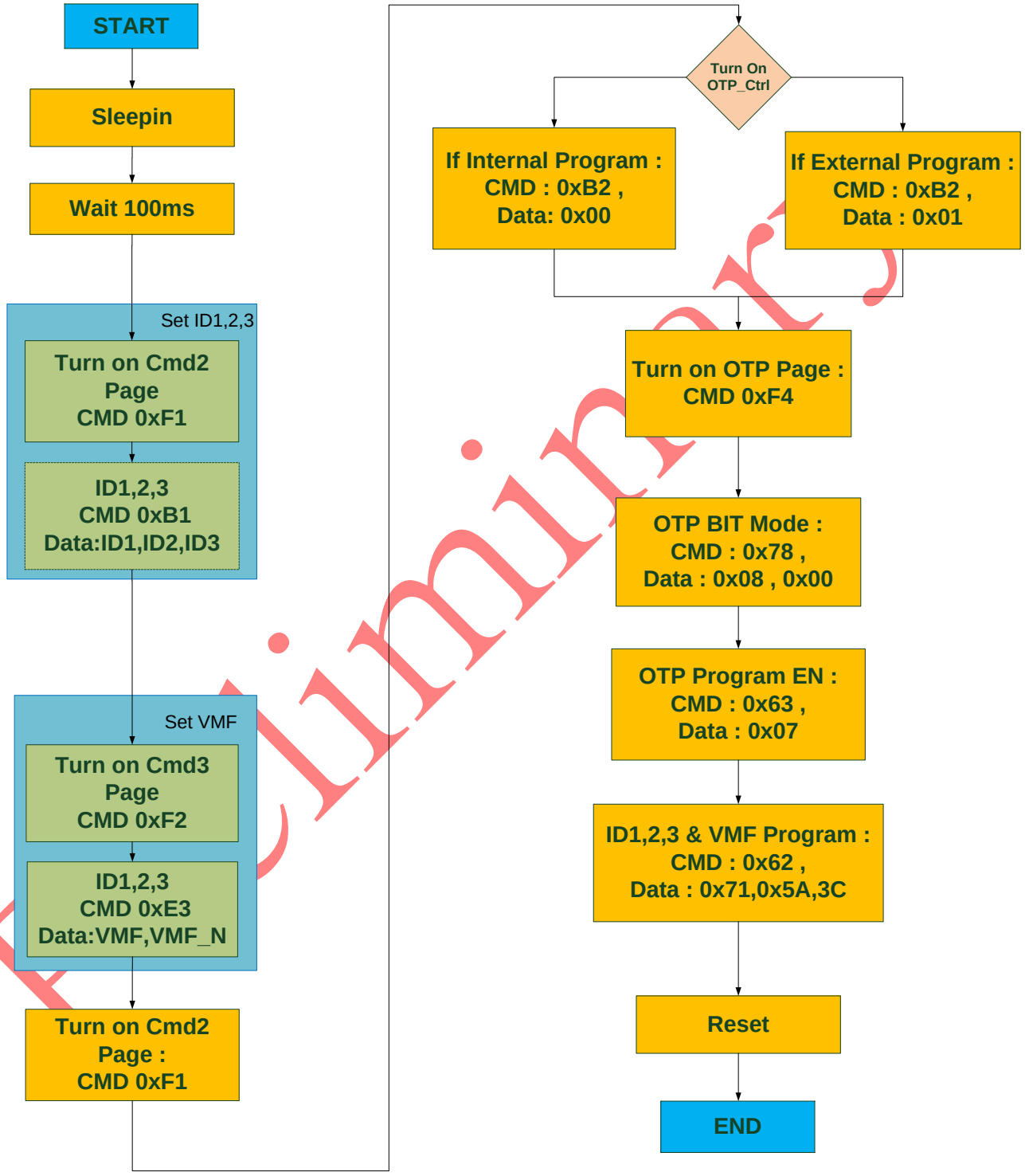
10.5 Voltage Generation



10.6 Relationship about source voltage

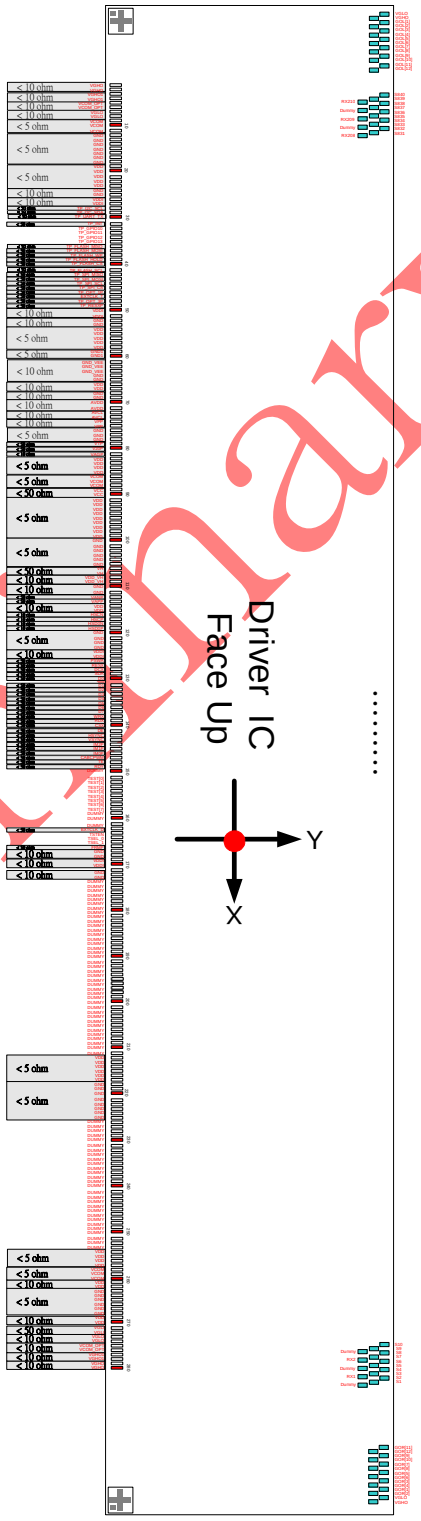


11 NVM PROGRAMMING FLOW



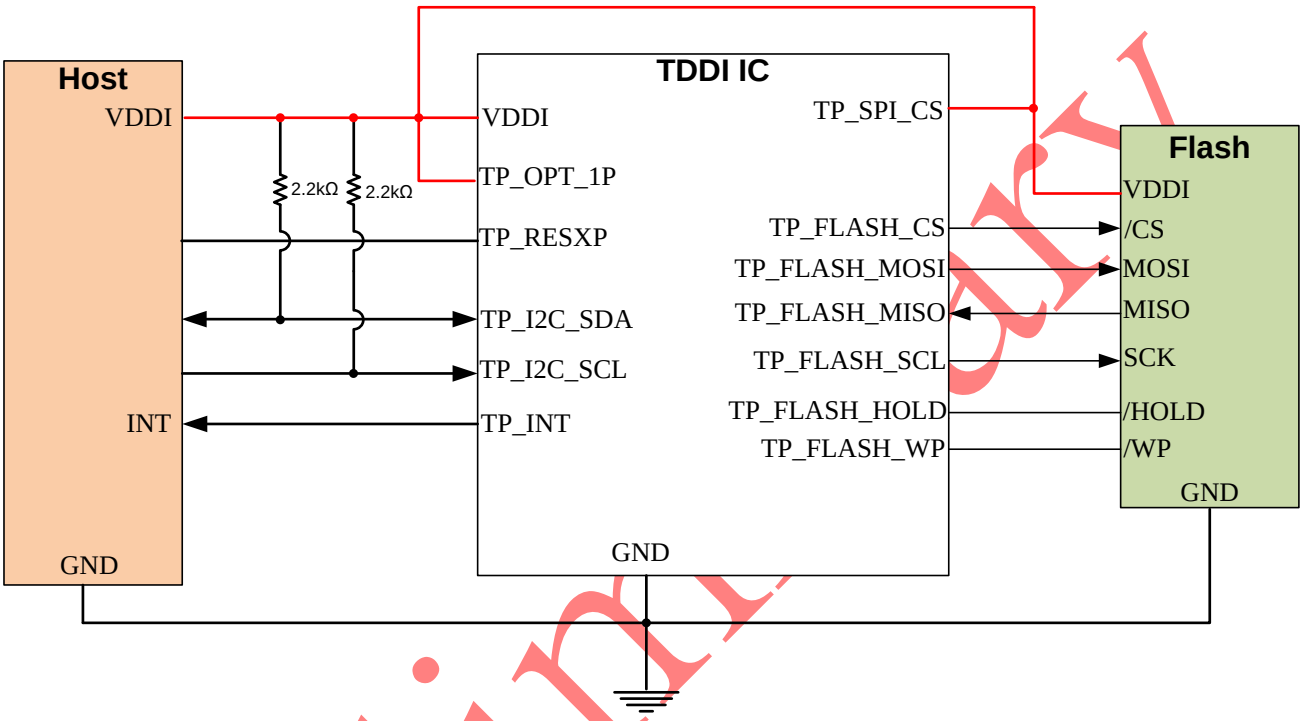
12 APPLICATION NOTE

12.1 Layout Resistance Suggestion

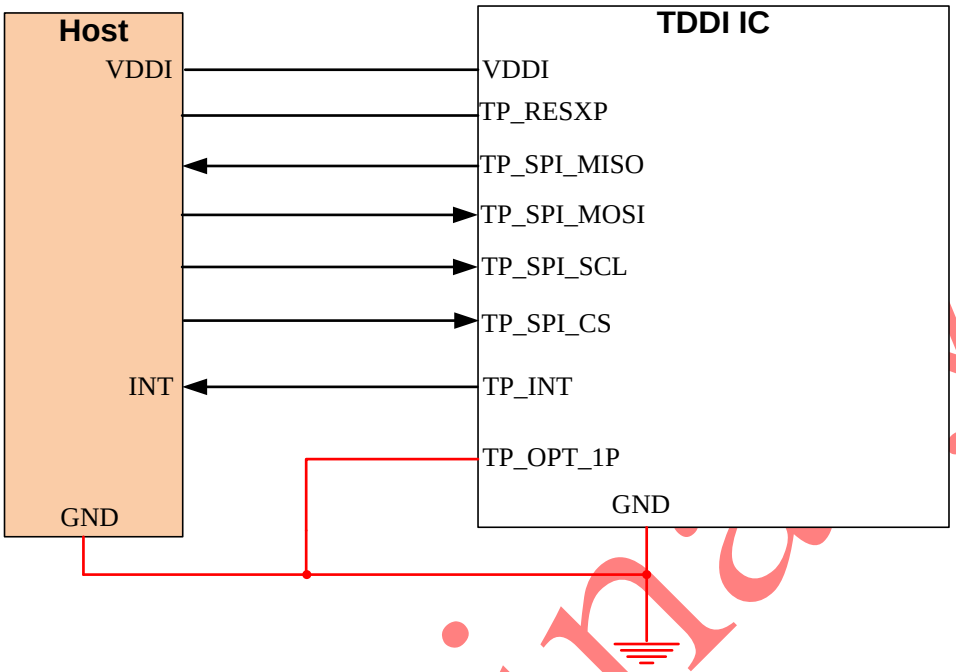


Touch Application circuit

12.2.1 With Flash Mode Application Circuit

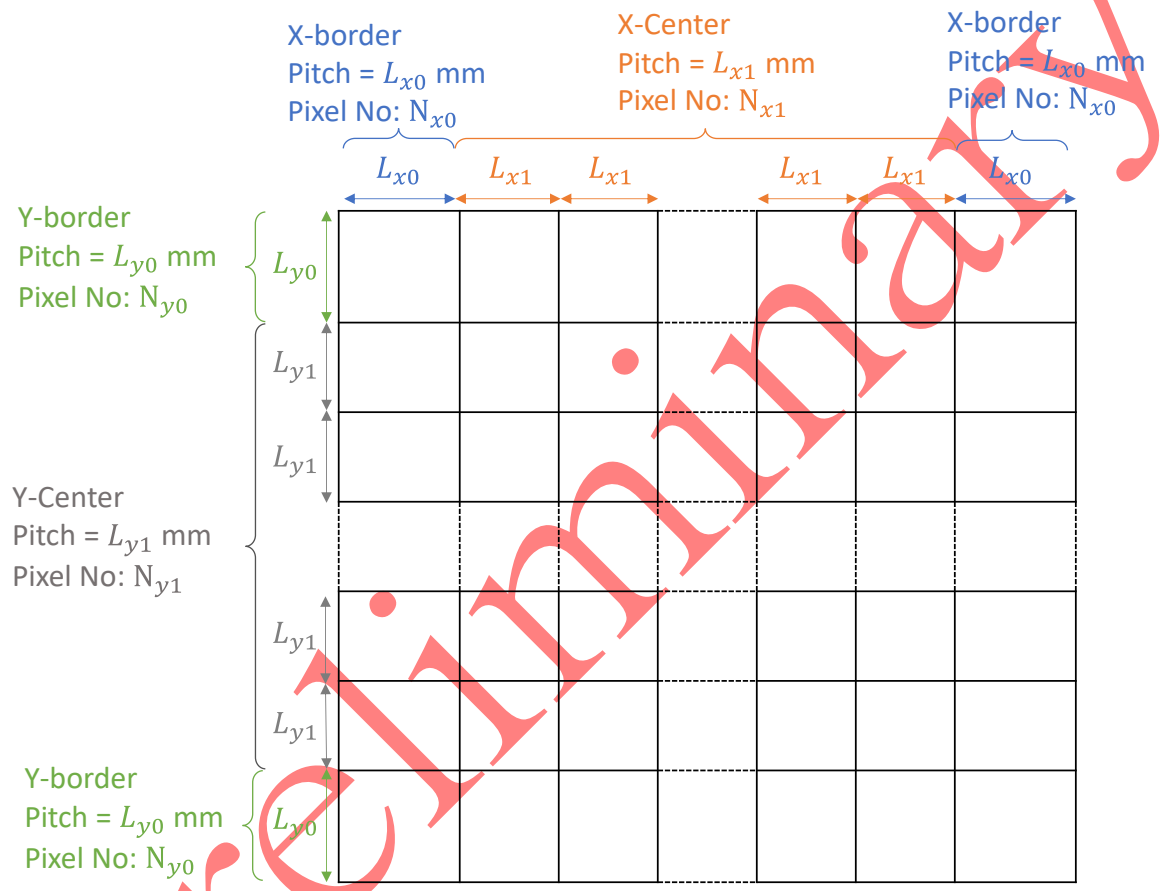


12.2.2 No-Flash Mode Application Circuit



12.3 Touch Electrode Application

The pitch of X-axis & Y-axis will be defined by two sizes, the leftmost channel and rightmost channel are the border channels and pitch should be the same. Others are the center channels where the pitch of center channels should be all the same which can be different pitches with border channels.



13 COMMAND

13.1 Page Set Table

PAGE SET Table													
Instruction	**D/CX**	**WRX**	**RDX**	**PNUM**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
SWCMD1	0	↑	1	-	1	1	1	1	0	0	0	0	(F0h)	Switch to CMD1
SWCMD2	0	↑	1	-	1	1	1	1	0	0	0	1	(F1h)	Switch to CMD2
SWCMD3	0	↑	1	-	1	1	1	1	0	0	1	1	(F2h)	Switch to CMD3

SWCMD1 (F0h): Switch to CMD1

F0H	Switch to CMD1												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SWCMD1	0	↑	1	-	1	1	1	1	0	0	0	0	(F0h)
Parameter	No Parameter												
Description	This command is used to select the function of Command 1												
Register availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

SWCMD2 (F1h): Switch to CMD2

F1H	Switch to CMD2												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CK	0	↑	1	-	1	1	1	1	0	0	0	1	(F1h)
Parameter	No Parameter												
Description	This command is used to select the function of Command 2												
Register availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

SWCMD3 (F2h): Switch to CMD3

F2H	Switch to CMD3												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CK	0	↑	1	-	1	1	1	1	0	0	1	0	(F2h)
Parameter	No Parameter												
Description	This command is used to select the function of Command 3												
Register availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

13.2 Command Table 1

COMMAND Table 1														
Instruction	**D/CX**	**WRX**	**RDX**	**PNUM**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)	No Operation
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software Reset
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read Display ID
	1	1	↑		-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		ID1[7:0]									ID1 read
	1	1	↑		ID2[7:0]									ID2 read
	1	1	↑		ID3[7:0]									ID3 read
RDNUMED	0	↑	1	-	0	0	0	0	0	1	0	1	(05h)	Read Number of Errors on DSI
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	DSI_ERR_NUM[7:0]									
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read Display Status
	1	1	↑		-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		MY	MX	-	ML	RGB	MH	-	-		
	1	1	↑		BSTON	-	IFPF[1:0]		IDMON	PTLON	SLOUT	NORON		
	1	1	↑		VSSON	-	INVON	-	-	DISON	TEON	-		
	1	1	↑		-	-	TELOM	-	-	-	-	-		
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read Display Power Mode
	1	1	↑		-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		BSTON	IDMON	PLTON	SLPOUT	NORON	DISON	-	-		
RDD MADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)	Read Display MADCTL
	1	1	↑		-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		MY	MX	-	ML	BGR	MH	-	-		
RDD COLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read Display Pixel Format
	1	1	↑		-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		-	-	-	-	-	-	IFPF.1-0			

COMMAND Table 1														
Instruction	**D/CX**	**WRX**	**RDX**	**PNUM**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read Display Image Mode
	1	1	↑		-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		VSSON	-	INVON	-	-	-	-	-		
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read Display Signal Mode
	1	1	↑		-	-	-	-	-	-	-	-	-	Dummy read
	1	1	↑		TEON	TELOM	-	-	-	-	-	EDSI		
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)	Read Display Sef-Diagnostic
	1	1	↑		-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		RLD	-	-	-	-	-	-	CCR		
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep in
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep out
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)	Partial On
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)	Normal On
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display inversion off
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display inversion on
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display off
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display on
CASET	0	↑	1	4	0	0	1	0	1	0	1	0	(2Ah)	Column Address Set
	1	↑	1		-	-	-	-	-	-	XS9	XS8		X address start: 0≦XS≦X
	1	↑	1		XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		
	1	↑	1		-	-	-	-	-	-	XE9	XE8		X address start: S≦XE≦X
	1	↑	1		XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		
RASET	0	↑	1	4	0	0	1	0	1	0	1	1	(2Bh)	Row Address Set
	1	↑	1		-	-	-	-	-	YS10	YS9	YS8		Y address start: 0≦YS≦Y
	1	↑	1		YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		

COMMAND Table 1														
Instruction	**D/CX**	**WRX**	**RDX**	**PNUM**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
	1	↑	1		-	-	-	-	-	-	YE9	YE8		Y address start: S≦YE≦Y
	1	↑	1		YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory Write
	1	↑	1		D1[7:0]									Write data
	1	↑	1		Dx[7:0]									
	1	↑	1		Dn[7:0]									
RAMRD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)	Memory Read
	1	1	↑		-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		D1[7:0]									Read data
	1	1	↑		Dx[7:0]									
	1	1	↑		Dn[7:0]									
RPLTAR	0	↑	1	4	0	0	1	1	0	0	0	0	(30h)	Partial Area
	1	1	↑		-	-	-	-	-	SR[10:8]				
	1	1	↑		SR[7:0]									
	1	1	↑		-	-	-	-	-	ER[10:8]				
	1	1	↑		ER[7:0]									
VSCRDEF	0	↑	1	6	0	0	1	1	0	0	1	1	(33h)	Vertical Scrolling Definition
	1	↑	1		-	-	-	-	-	TFA[10:8]				
	1	↑	1		TFA[7:0]									
	1	↑	1		-	-	-	-	-	VSA[10:8]				
	1	↑	1		VSA[7:0]									
	1	↑	1		-	-	-	-	-	BFA[10:8]				
	1	↑	1		BFA[7:0]									
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing Effect Line off
TEON	0	↑	1	1	0	0	1	1	0	1	0	1	(35h)	Tearing Effect Line on
	1	↑	1		-	-	-	-	-	-	-	TELO		
MADCTL	0	↑	1	1	0	0	1	1	0	1	1	0	(36h)	Memory Data Access Control
	1	↑	1		MY	MX	-	ML	RGB	MH	-	-		
VSCRSADD	0	↑	1	2	0	0	1	1	0	1	1	1	(37h)	Vertical Scrolling Start Address
	1	↑	1		-	-	-	-	-	VSP[10:8]				
	1	↑	1		VSP[7:0]									
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle Mode off

COMMAND Table 1														
Instruction	**D/CX**	**WRX**	**RDX**	**PNUM**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle Mode on
COLMOD	0	↑	1	1	0	0	1	1	1	0	1	0	(3Ah)	Interface Pixel Format
	1	↑	1		-	-	-	-	-	-	IFPF[1:0]			
RAMWRC	0	↑	1	-	0	0	1	1	1	1	0	0	(3Ch)	Memory Write Continue
	1	↑	1		D1[7:0]									Write data
	1	↑	1		Dx[7:0]									
	1	↑	1		Dn[7:0]									
RAMRDC	0	↑	1	-	0	0	1	1	1	1	1	0	(3Eh)	Memory Write Continue
	1	1	↑		-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		D1[7:0]									Read data
	1	1	↑		Dx[7:0]									
	1	1	↑		Dn[7:0]									
SPIRDMD	0	↑	1	-	0	0	1	1	0	0	1	1	(42h)	SPI Read Mode
	1	↑	1		SPI_RD_CAP[7:0]									
TESLWR	0	↑	1	2	0	1	0	0	0	1	0	0	(44h)	Write Tear Scan Line
	1	↑	1		-	-	-	-	TE_SL[11:8]					
	1	↑	1		TE_SL[7:0]									
TESLRD	0	↑	1	2	0	1	0	0	0	1	0	1	(45h)	Read Tear Scan Line
	1	1	↑		-	-	-	-				-		Dummy Read
	1	1	↑		-	-	-	-	TE_SL[11:8]					
	1	1	↑		TE_SL[7:0]									
RAMCLACT	0	↑	1	-	0	1	0	0	1	1	0	0	(4Ch)	Memory Clear Act
RAMCLRSET	0	↑	1	3	0	1	0	0	1	1	0	1	(4Dh)	Memory Clear Setting
	1	↑	1		CLNRAM_R[7:0]									
	1	↑	1		CLNRAM_G[7:0]									
	1	↑	1		CLNRAM_B[7:0]									
RAMCLRBUSY	0	↑	1	-	0	1	0	0	1	1	1	0	(4Eh)	Memory Clear Busy
	1	1	↑		-	-	-	-	-	-	-	-		Dummy Read

COMMAND Table 1														
Instruction	**D/CX**	**WRX**	**RDX**	**PNUM**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
	1	1	↑		-	-	-	-	-	-	-	CLR_BUSY		
DSTB	0	↑	1	-	0	1	0	0	1	1	1	1	(4Fh)	Deep Standby
	1	↑	1		-	-	-	-	-	-	-	DSTB		Mode
WRDISBV	0	↑	1	-	0	1	0	1	0	0	0	1	(51h)	Write Display
	1	↑	1		DBV[7:0]									Brightness
RDDISBV	0	↑	1	-	0	1	0	1	0	0	1	0	(52h)	Read Display Brightness
	1	1	↑		-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		DBV[7:0]									
WRCTRLD	0	↑	1	1	0	1	0	1	0	0	1	1	(53h)	Write CTRL
	1	↑	1		-	-	-	-	-	BL	-	-		Display
RDCTRLD	0	↑	1	-	0	1	0	1	0	1	0	0	(54h)	Read CTRL Display
	1	1	↑		-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		-	-	-	-	-	BL	-	-		
WRSRECTRL	0	↑	1	1	0	1	0	1	0	1	0	1	(55h)	Write Content Adaptive Brightness Control
	0	↑	1		-	SRE_EN	-	-	-	-	-	-		
RDSRECTRL	0	↑	1	-	0	1	0	1	0	1	1	0	(56h)	Read Content Adaptive Brightness Control
	1	1	↑		-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		-	SRE_EN	-	-	-	-	-	-		
RDFCS	0	↑	1	-	0	1	1	0	1	1	0	0	(AAh)	Read First Checksum
	1	1	↑											Dummy read
	1	1	↑		FCS[7:0]									

COMMAND Table 1														
Instruction	**D/CX**	**WRX**	**RDX**	**PNUM**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
RDCCS	0	↑	1	-	0	1	1	0	1	1	0	1	(AFh)	Read Continuous Checksum
	1	1	↑											Dummy read
	1	1	↑		CCS[7:0]									
RAMMD	0	↑	1	1	0	1	1	0	1	1	1	1	(D0h)	RAM Mode
	1	↑	1		Scan_ram_spwr	-	-	-	-	-	Video_mode[1:0]			
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)	Read ID1
	1	1	↑		-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		ID1[7:0]									
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
	1	1	↑		-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		ID2[7:0]									
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3
	1	1	↑		-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		ID3[7:0]									

NOP (00h)

00H	NOP (No Operation)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)
Parameter	No Parameter												-
Description	This command is empty command. "-" Don't care												
Restriction													

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart

SWRESET (01h): Software Reset

01H	SWRESET (Software Reset)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)
Parameter	No Parameter												-
Description	"-" Don't care - When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. - Frame memory contents are unaffected by this command.												
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during this 5msec. If software reset is sent during sleep in mode, it will be necessary to wait 120msec before sending sleep out command. Software reset command cannot be sent during sleep out sequence.												

Register Availability

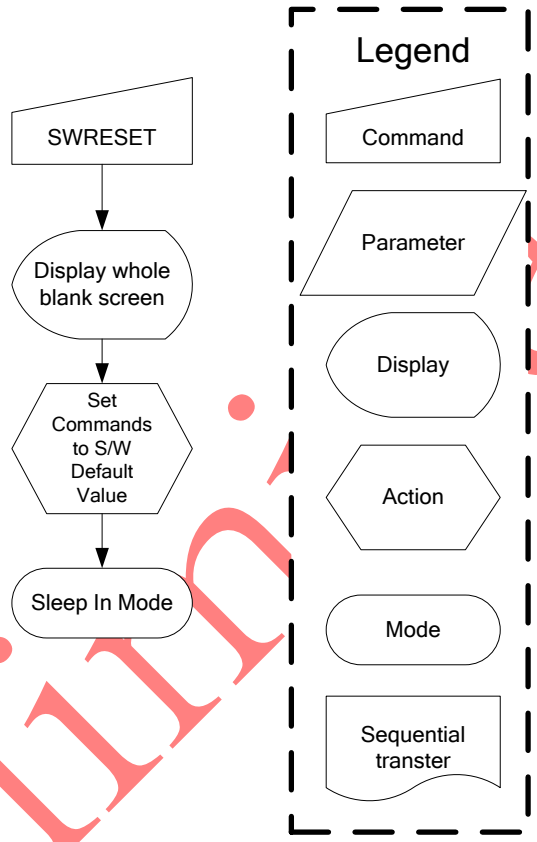
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes

	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart



RDDID (04h): Read Display ID

04H	RDDID (Read Display ID)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-		ID1[6:0]							
3rd parameter	1	1	↑	-		ID2[6:0]							
4th parameter	1	1	↑	-		ID3[6:0]							
Description	-This read byte returns 24-bit display identification information. -The 1st parameter is dummy data -The 2nd parameter (ID1[6:0]): LCD module's manufacturer ID. -The 3rd parameter (ID2[6:0]): LCD module/driver version ID -The 4th parameter (ID3[6:0]): LCD module/driver ID. -Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively. "-" Don't care												
Restriction													

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	See description	See description	See description
S/W Reset	See description	See description	See description
H/W Reset	See description	See description	See description

RDDST (09h): Read Display Status

09H	RDDST (Read Display Status)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	MY	MX	-	ML	RGB	MH	-	-	
3rd parameter	1	1	↑	-	BOTON	-	IFPF[1:0]		IDMON	PTLON	SLOUT	NORON	

4th parameter	1	1	↑	-	VSSON	-	INVON	-	-	DISON	TEON	-	
5th parameter	1	1	↑	-	-	-	TELOM	-	-	-	-	-	

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off
MY	Row Address Order (MY)	'1' =Decrement, (Bottom to Top, when MADCTL (36h) D7='1') '0' =Increment, (Top to Bottom, when MADCTL (36h) D7='0')
MX	Column Address Order (MX)	'1' =Decrement, (Right to Left, when MADCTL (36h) D6='1') '0' =Increment, (Left to Right, when MADCTL (36h) D6='0')
ML	Scan Address Order (ML)	'0' =Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4='0') '1'=Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4='1')
RGB	RGB/ BGR Order (RGB)	'1' =BGR, (When MADCTL (36h) D3='1') '0' =RGB, (When MADCTL (36h) D3='0')
MH	Horizontal Order	'0' =Decrement, (LCD refresh Left to Right, when MADCTL (36h) D2='0') '1' =Increment, (LCD refresh Right to Left, when MADCTL (36h) D2='1')
IFPF[1:0]	Interface Color Pixel Format Definition	"01" = 16-bit / pixel, "10" = 18-bit / pixel, "11" = 24-bit / pixel, others are not defined.
IDMON	Idle Mode On/Off	'1' = On, "0" = Off
SLPOUT	Sleep In/Out	'1' = Out, "0" = In
NORON	Display Normal Mode On/Off	'1' = Normal Display,
INVON	Inversion Status	'1' = On, "0" = Off
DISON	Display On/Off	'1' = On, "0" = Off
TEON	Tearing effect line on/off	'1' = On, "0" = Off
TELOM	Tearing effect line mode	'0' = mode1, '1' = mode2

"-" Don't care

RDDPM (0Ah): Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	-	(0Ah)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	BSTON	IDMON	PLTON	SLPOUT	NORON	DISON	-	-	

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off
IDMON	Idle mode on/off	'1' = Idle Mode On, '0' = Idle Mode Off
PTLON	Partial mode on/off	'1' =Partial mode on, '0' =Partial mode off,
SLPOUT	Sleep in/out	'1' =Sleep out, '0' =Sleep in,
NORON	Display normal mode on/off	'1' = Normal display, '0' = Partial display,
DISON	Display on/off	'1' =Display on, '0' =Display off,

"-" Don't care

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000-1000(08h)
S/W Reset	0000-1000(08h)
H/W Reset	0000-1000(08h)

RDDMADCTL (0Bh): Read Display MADCTL

0BH	RDDMADCTL (Read Display MADCTL)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDMADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	MY	MX	-	ML	RGB	MH	-	-	

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
MY	Row Address Order (MY)	'1' =Decrement, (Bottom to Top, when MADCTL (36h) D7='1') '0' =Increment, (Top to Bottom, when MADCTL (36h) D7='0')

	MX	Column Address Order (MX)	‘1’ =Decrement, (Right to Left, when MADCTL (36h) D6=’1’) ‘0’ =Increment, (Left to Right, when MADCTL (36h) D6=’0’)
	ML	Scan Address Order (ML)	‘0’ =Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4=’0’) ‘1’=Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4=’1’)
	RGB	RGB/ BGR Order (RGB)	‘1’ =BGR, (When MADCTL (36h) D3=’1’) ‘0’ =RGB, (When MADCTL (36h) D3=’0’)
	MH	Horizontal Order	‘0’ =Decrement, (LCD refresh Left to Right, when MADCTL (36h) D2=’0’) ‘1’ =Increment, (LCD refresh Right to Left, when MADCTL (36h) D2=’1’)

“-“ Don’t care

Restriction	There is one dummy parameter when using Parallel interface.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000-0000 (00h)
S/W Reset	No change
H/W Reset	0000-0000 (00h)

RDDCOLMOD (0Ch): Read Display Pixel Format

<table>
<tr><td>0CH</td><td colspan="13">RDDCOLMOD (Read Display Pixel Format)</td></tr>
<tr><td>Inst / Para</td><td>D/CX</td><td>WRX</td><td>RDX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>RDDCOLMOD</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>(0Ch)</td></tr>
<tr><td>1st parameter</td><td>1</td><td>1</td><td>↑</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>1</td><td>↑</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td colspan="3">IFPF[1:0]</td><td></td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table><tr><td>Bit</td><td>Description</td><td>Value</td></tr><tr><td>IFPF[1:0]</td><td>Control interface color format</td><td>‘01’ = 16 bit/pixel
‘10’ = 18 bit/pixel
‘11’ = 24 bit/pixel</td></tr></table>
“-“ Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">There is one dummy parameter when using Parallel interface.</td></tr>
<tr><td>Register availability</td><td colspan="13"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>0000-0011 (24 bit/pixel)</td></tr><tr><td>S/W Reset</td><td>No change</td></tr><tr><td>H/W Reset</td><td>0000-0011 (24 bit/pixel)</td></tr></table></td></tr>
</table>

RDDIM (0Dh): Read Display Image Mode

0DH	RDDIM (Read Display Image Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	VSSON	-	INVON	-	-	-	-	-	
Description	This command indicates the current status of the display as described in the table below: -VSSON: Vertical scrolling on/off -INVON: Inversion on/off Others are no define and invalid "-" Don't care												
Restriction	There is one dummy parameter when using Parallel interface.												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000-0000
S/W Reset	0000-0000
H/W Reset	0000-0000

RDDSM (0Eh): Read Display Signal Mode

0EH	RDDSM (Read Display Signal Status)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	TEON	TELOM	-	-	-	-	-	EDSI	

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
TEON	Tearing effect line on/off	'1' = ON, '0' = OFF,
TELOM	Tearing effect line mode	'1' = mode2, '0' = mode1,
EDSI	Error on DSI	'1' = Error, '0' = No Error,

	"-" Don't care
Restriction	There is one dummy parameter when using Parallel interface.
Register availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000-0000
S/W Reset	0000-0000
H/W Reset	0000-0000

RDDSDR (0Fh): Read Display Self-Diagnostic Result

0FH	RDBST (Read Busy Status)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDBST	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	RLD	-	-	-	-	-	-	CCR	

Description

This command indicates the current status of the display as described in the table below:

-RLD: This bit is the Register Loading Detection

-CCR: The cmd1 checksum compare result.

0 = Checksum is the same.

1 = Checksum is not the same

"-" Don't care

Restriction: There is one dummy parameter when using Parallel interface.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000-0000
S/W Reset	0000-0000
H/W Reset	0000-0000

SLPIN (10h): Sleep in

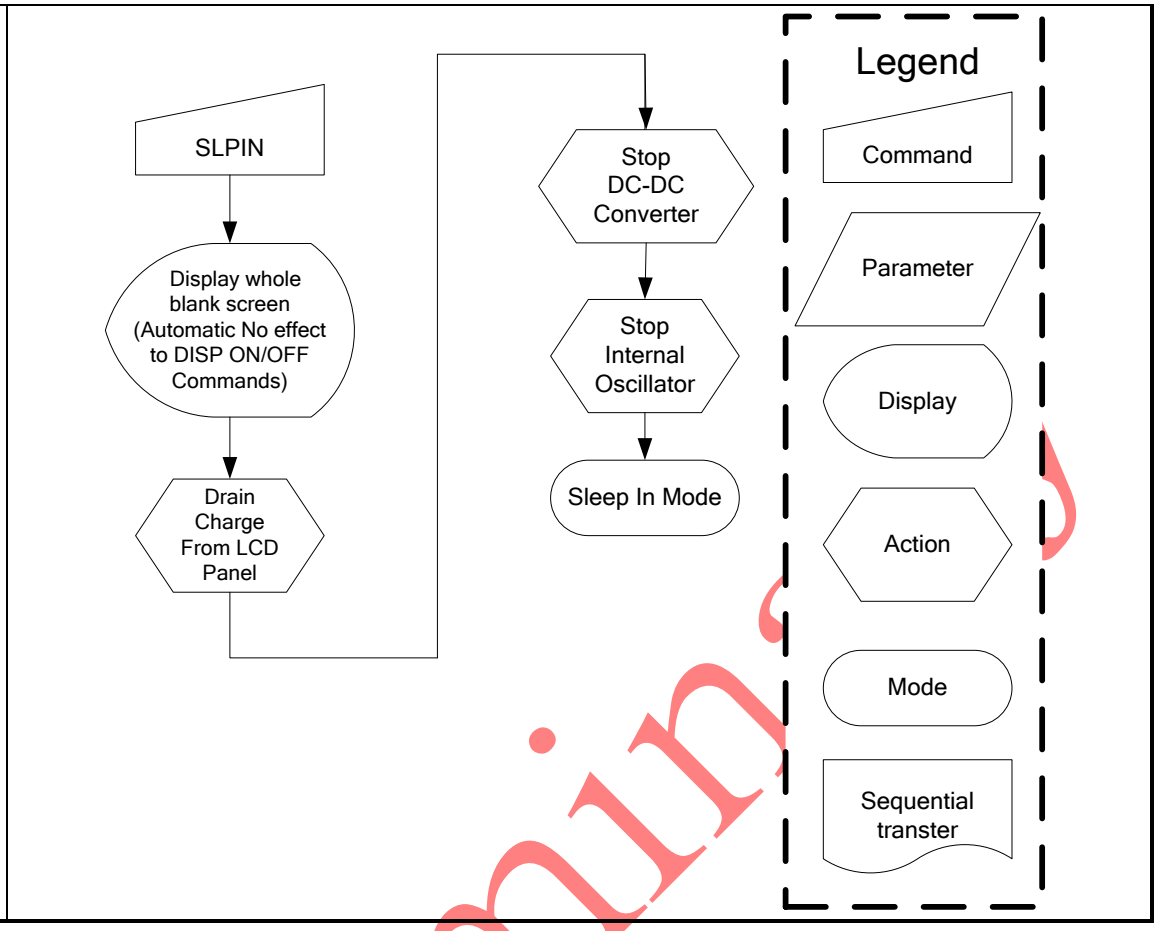
10H	SLPIN (Sleep In)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)
parameter	No Parameter												
Description	-This command causes the LCD module to enter the minimum power consumption mode. -In this mode the DC/DC converter is stopped, internal oscillator is stopped, and panel scanning is stopped. -MCU interface and memory are still working and the memory keeps its contents. -Dimming function does not work when there is changing mode from Sleep OUT to Sleep IN. "-" Don't care												
Restriction	-This command has no effect when module is already in sleep in mode. Sleep in mode can only be left by the sleep out command (11h). -It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize. -It will be necessary to wait 120msec after sending sleep out command (when in sleep in mode) before sending an sleep in command.												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Flow Chart	

SLPOUT (11h): Sleep Out

11H	SLPOUT (Sleep Out)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)
parameter	No Parameter												
Description	-This command turn off sleep mode. -In this mode the DC/DC converter is enabled, internal display oscillator is started, and panel scanning is started.												
Restriction	-This command has no effect when module is already in sleep out mode. Sleep out mode can only be left by the sleep in command (10h). -It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize. -It will be necessary to wait 120msec after sending sleep out command (when in sleep in mode) before sending an sleep in command. -The display module runs the self-diagnostic functions after this command is received.												

Register availability

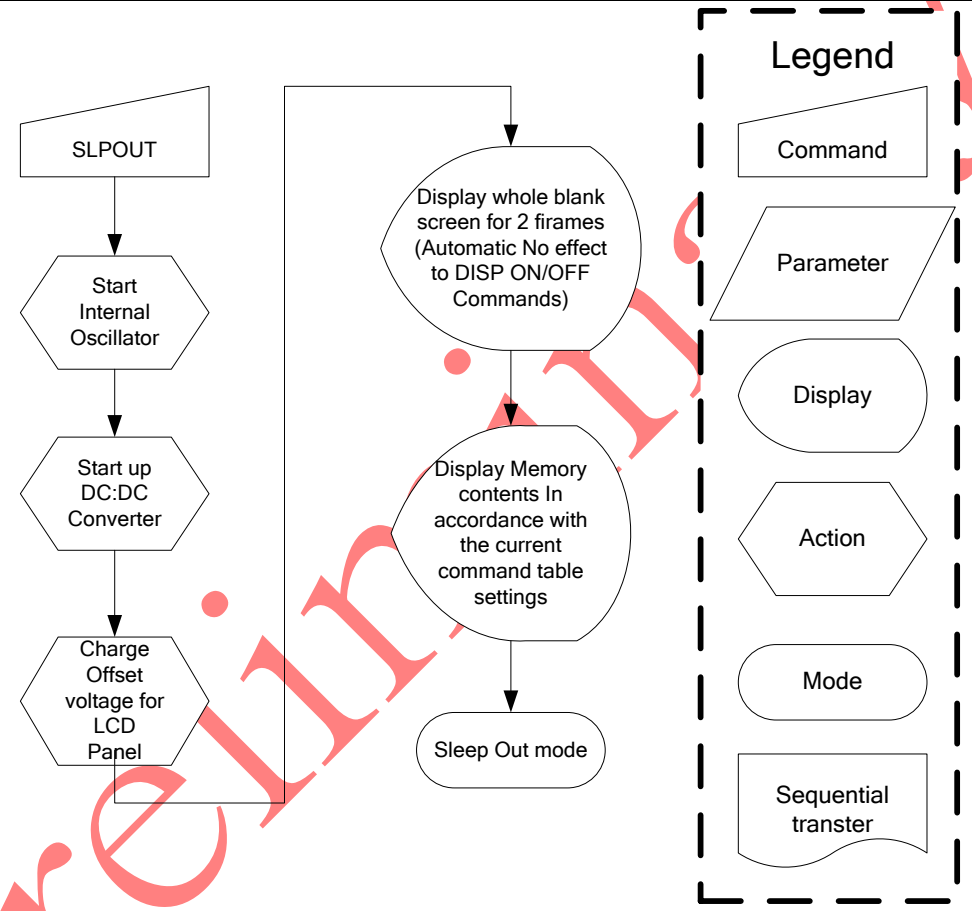
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes

	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Flow Chart



PTLON (12h): Partial Display Mode On

12H	PTLON (Partial Display Mode on)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)
parameter	No Parameter												
Description	-This command turns on Partial mode. The Partial mode window us described by the Partial Area (30h,31h). -To leave Partial mode, the Normal Display Mode On command (13h) should be written. "-" Don't care												
Restriction	This command has no effect when partial mode is active.												
Register													

<table>
<tr><td>availability</td><td></td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Normal display mode on</td></tr>
<tr><td>S/W Reset</td><td>Normal display mode on</td></tr>
<tr><td>H/W Reset</td><td>Normal display mode on</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Partial Area (30h/31h)</td></tr>
</table>

NORON (13h): Normal On

12H	NORON (Normal On)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)
parameter	No Parameter												
Description	-This command turns the display to Normal On mode. -Normal display mode on means Normal off mode off. -Exit from NORON by the NOROFF command. "-" Don't care												
Restriction	This command has no effect when Normal On mode is active.												
Register availability													

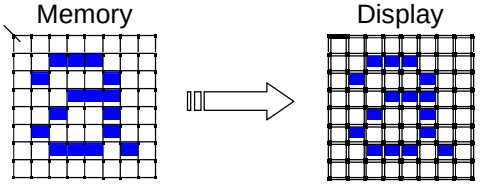
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

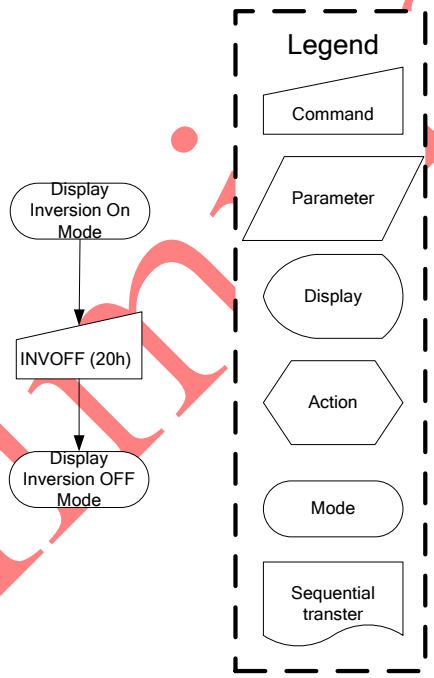
Default

Status	Default Value
Power On Sequence	Normal display mode on
S/W Reset	Normal display mode on
H/W Reset	Normal display mode on

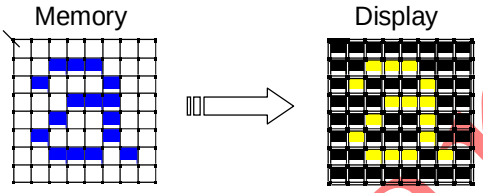
Flow Chart

INVOFF (20h): Display Inversion Off

20H	INVOFF (Display Inversion Off)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)
parameter	No Parameter												
Description	-This command is used to recover from display inversion mode. "-" Don't care (Example) Top-Left (0,0) Memory Display 												

<table>
<tr><td>Restriction</td><td>This command has no effect when module is already in inversion off mode.</td></tr>
<tr><td>Register availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Display inversion off</td></tr>
<tr><td>S/W Reset</td><td>Display inversion off</td></tr>
<tr><td>H/W Reset</td><td>Display inversion off</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

INVON (21h): Display Inversion On

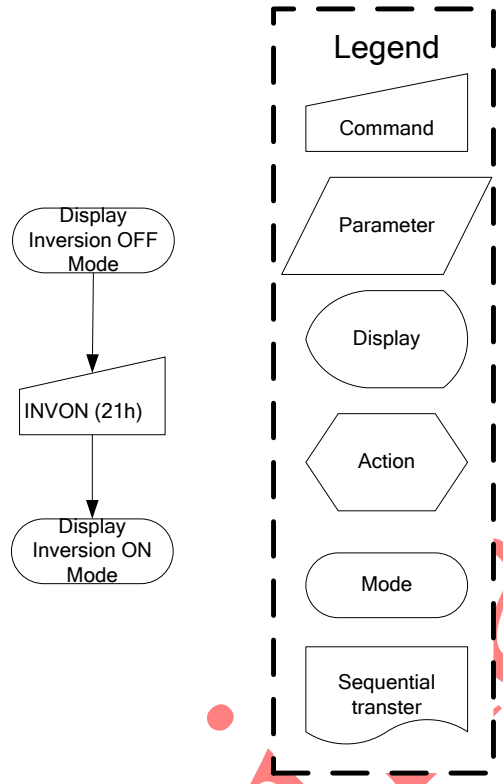
21H	INVON (Display Inversion On)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)
parameter	No Parameter												
Description	-This command is used to recover from display inversion mode. "-" Don't care (Example) Top-Left (0,0) Memory → Display 												
Restriction	This command has no effect when module is already in inversion on mode.												

Register availability

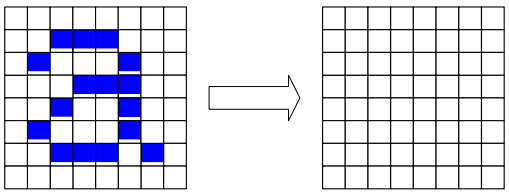
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display inversion off
S/W Reset	Display inversion off
H/W Reset	Display inversion off

Flow Chart	

DISPOFF (28h): Display Off

28H	DISPOFF (Display Off)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)
parameter	No Parameter												
Description	- This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. - This command makes no change of contents of frame memory. - This command does not change any other status. - There will be no abnormal visible effect on the display. - Exit from this command by Display On (29h) **(Example)** **Memory** **Display** 												
Restriction	This command has no effect when module is already in display off mode.												

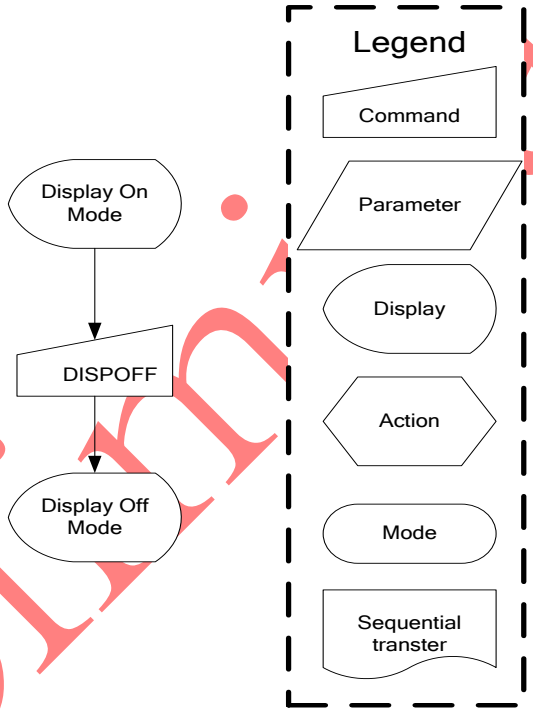
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

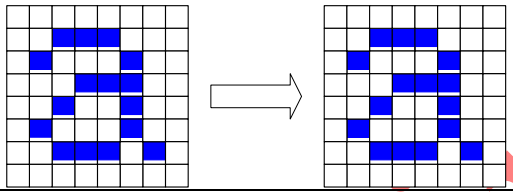
Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



DISPON (29h): Display On

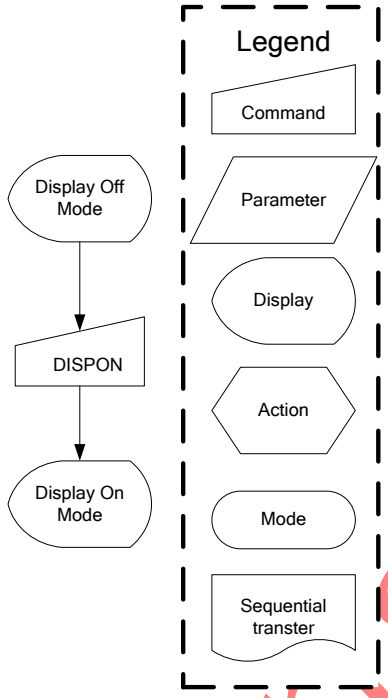
29H	DISPON (Display On)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPO N	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)
parameter	No Parameter												
Description	- This command is used to recover from DISPLAY OFF mode. - Output from the Frame Memory is enabled. - This command makes no change of contents of frame memory. - This command does not change any other status. **(Example)** **Memory** → **Display** 												
Restriction	This command has no effect when module is already in display on mode.												

Register availability

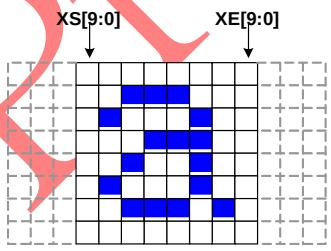
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart	

CASET (2Ah): Column Address Set

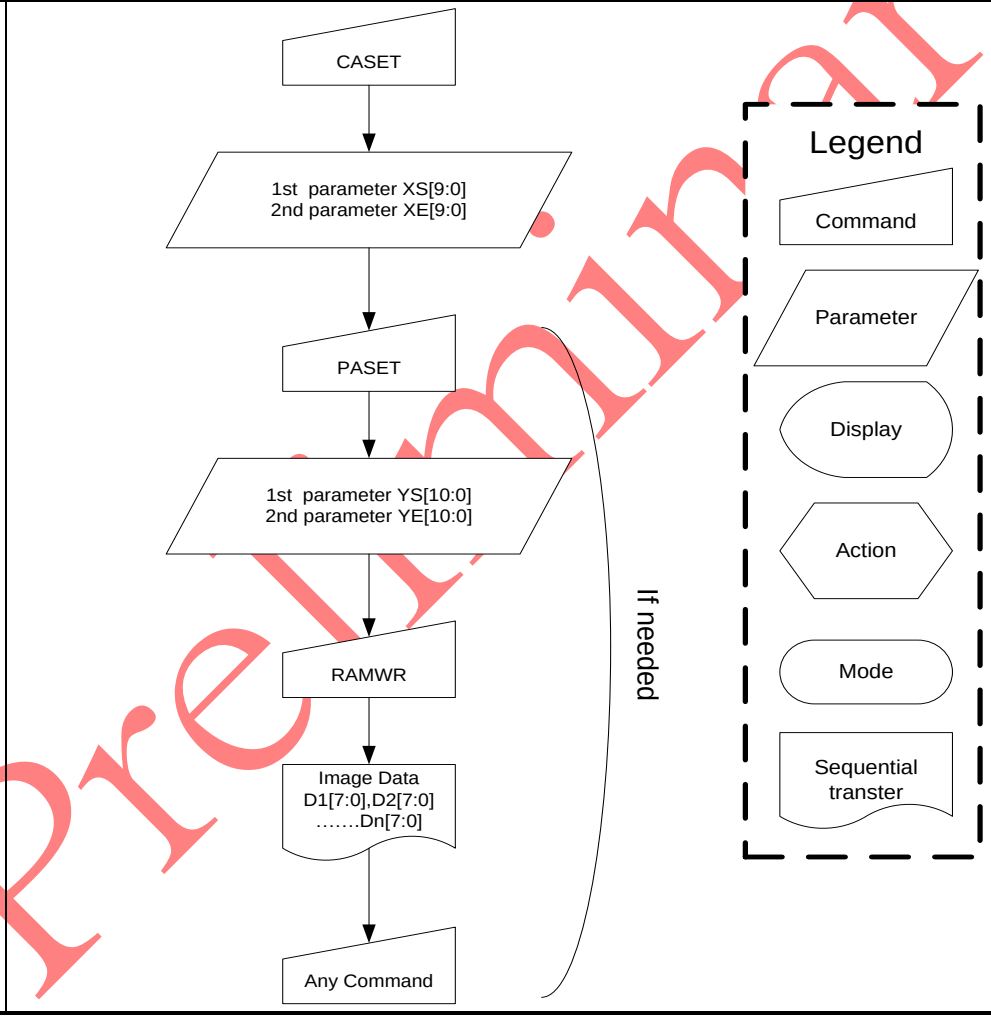
2AH	CASET (Column Address Set)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CASET	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)
1st parameter	1	↑	1	-	-	-	-	-	-	-	XS[9:8]		
2nd parameter	1	↑	1	-	XS[7:0]								
3rd parameter	1	↑	1	-	-	-	-	-	-	-	XE[9:8]		
4th parameter	1	↑	1	-	XE[7:0]								
Description	-The value of XS [9:0] and XE [9:0] are referred when RAMWR command comes. -Each value represents one column line in the Frame Memory. 												
Restriction	XS [9:0] always must be equal to or less than XE [9:0] When XS [9:0] or XE [9:0] is greater than maximum address like below, data of out of range will be ignored. (Parameter range: 0 < XS [9:0] < XE [9:0] < 559 (022Fh)): MV="0") (Parameter range: 0 < XS [9:0] < XE [9:0] < 559 (022Fh)): MV="1")												
Register availability	Status | Availability												

	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	XS[9:0]=0000h	XE[9:0]=0243h
S/W Reset	XS[9:0]=0000h	When MV=0: XE[9:0]=0243h When MV=1: XE[9:0]=0243h
H/W Reset	XS[9:0]=0000h	XE[9:0]=0243h

Flow Chart



RASET (2Bh): Row Address Set

2BH	RASET (Row Address Set)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RASET	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)
1st parameter	1	↑	1	-	-	-	-	-	-	YS[10:8]			

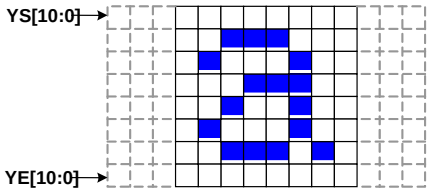
2nd parameter	1	↑	1	-	YS[7:0]						
3rd parameter	1	↑	1	-	-	-	-	-	-	YE[10:8]	
4th parameter	1	↑	1	-	YE[7:0]						

Description

-This command is used to define area of frame memory where MCU can access.

-The value of YS [10:0] and YE [10:0] are referred when RAMWR command comes.

-Each value represents one page line in the Frame Memory.



Restriction

YS [10:0] always must be equal to or less than YE [9:0]

When YS [10:0] or YE [10:0] is greater than maximum address like below, data of out of range will be ignored.

(Parameter range: 0 < YS [10:0] < YE [10:0] < 1023 (03FFh)): MV="0")

(Parameter range: 0 < YS [10:0] < YE [10:0] < 1023 (03FFh)): MV="1")

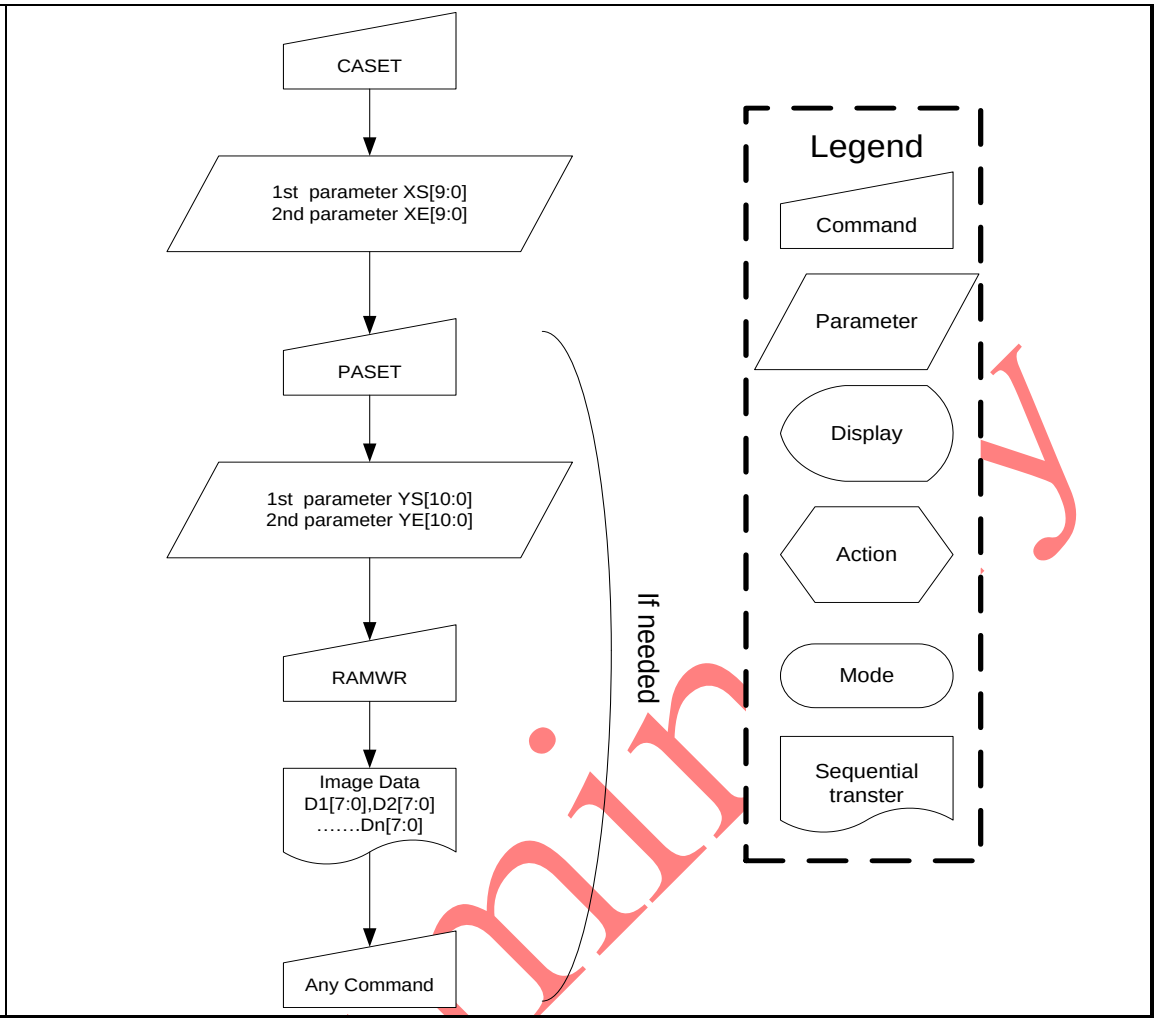
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	YS[10:0]=0000h	YE[10:0]=0243h
S/W Reset	YS[10:0]=0000h	When MV=0: YE[10:0]=0243h, When MV=1: YE[10:0]=0243h
H/W Reset	YS[10:0]=0000h	YE[10:0]=0243h

Flow Chart



RAMWR (2Ch): Memory Write

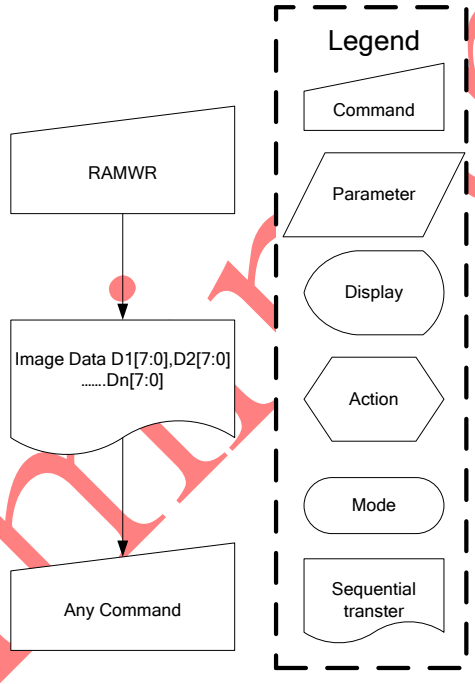
2CH	RAMWR (Memory Write)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)
1st parameter	1	↑	1	-	D1[7:0]								-
…	1	↑	1	-	.								-
N parameter	1	↑	1	-	Dn[7:0]								-
Description	-This command is used to transfer data from MCU to frame memory. -When this command is accepted, the column register and the page register are reset to the start column/start page positions. -The start column/start page positions are different in accordance with MADCTL setting. -Sending any other command can stop frame write.												
Restriction	In all color modes, there is no restriction on length of parameters.												
Register availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes												

Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

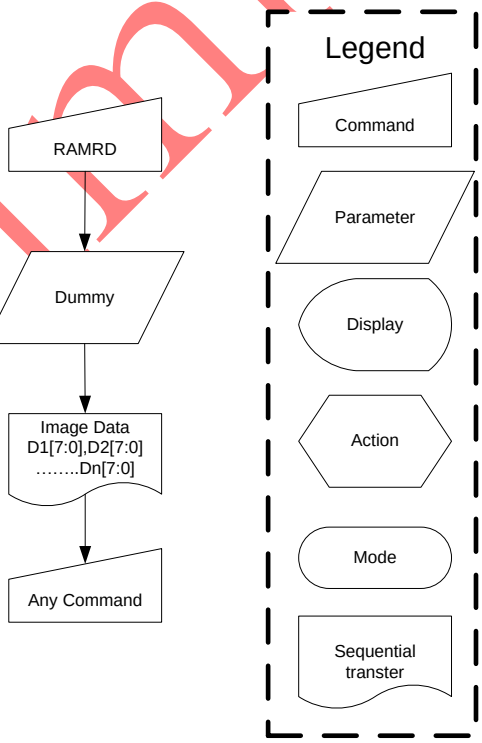
Flow Chart



RAMRD (2Eh): Memory Read

2CH	RAMRD (Memory Read)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMRD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D1[7:0]								-
:	1	1	↑	:	:								:
(N+1)th parameter	1	1	↑	-	Dn[7:0]								-
Description	-This command is used to transfer data from frame memory to MCU. -When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. -The Start Column/Start Row positions are different in accordance with MADCTL setting. -Then D[7:0] is read back from the frame memory and the column register and the row register incremented												

<table>
<tr><td></td><td>-Frame Read can be cancelled by sending any other command.
-The data color coding is fixed to 18-bit in reading function. Please see section 9.8 “Data color coding” for color coding (18-bit cases), when there is used 8, 9 data lines for image data.

Note1: The Command 3Ah should be set to 66h when reading pixel data from frame memory.</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr>
<tr><td>S/W Reset</td><td>Contents of memory is not cleared</td></tr>
<tr><td>H/W Reset</td><td>Contents of memory is not cleared</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

RPTLAR (30h): Partial Area

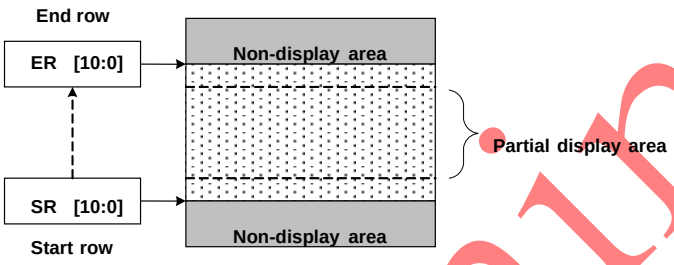
30H	PTLAR (Partial Area)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)
1st parameter	1	↑	1	-	-	-	-	-	-	SR[10:8]			
2nd parameter	1	↑	1	-	SR[7:0]								
3rd parameter	1	↑	1	-	-	-	-	-	-	ER[10:8]			
4th parameter	1	↑	1	-	ER[7:0]								

Description

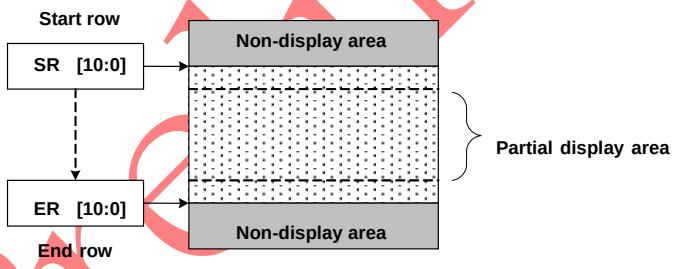
-This command defines the partial mode's display area.

-There are 4 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.

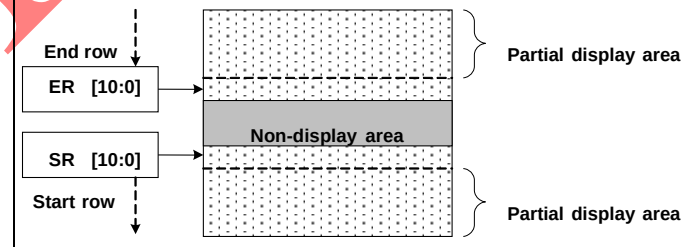
-If End Row > Start Row, when MADCTL ML='1'



-If End Row > Start Row, when MADCTL ML='0'



-If End Row < Start Row, when MADCTL ML='0'



-If End Row = Start Row then the Partial Area will be one row deep.

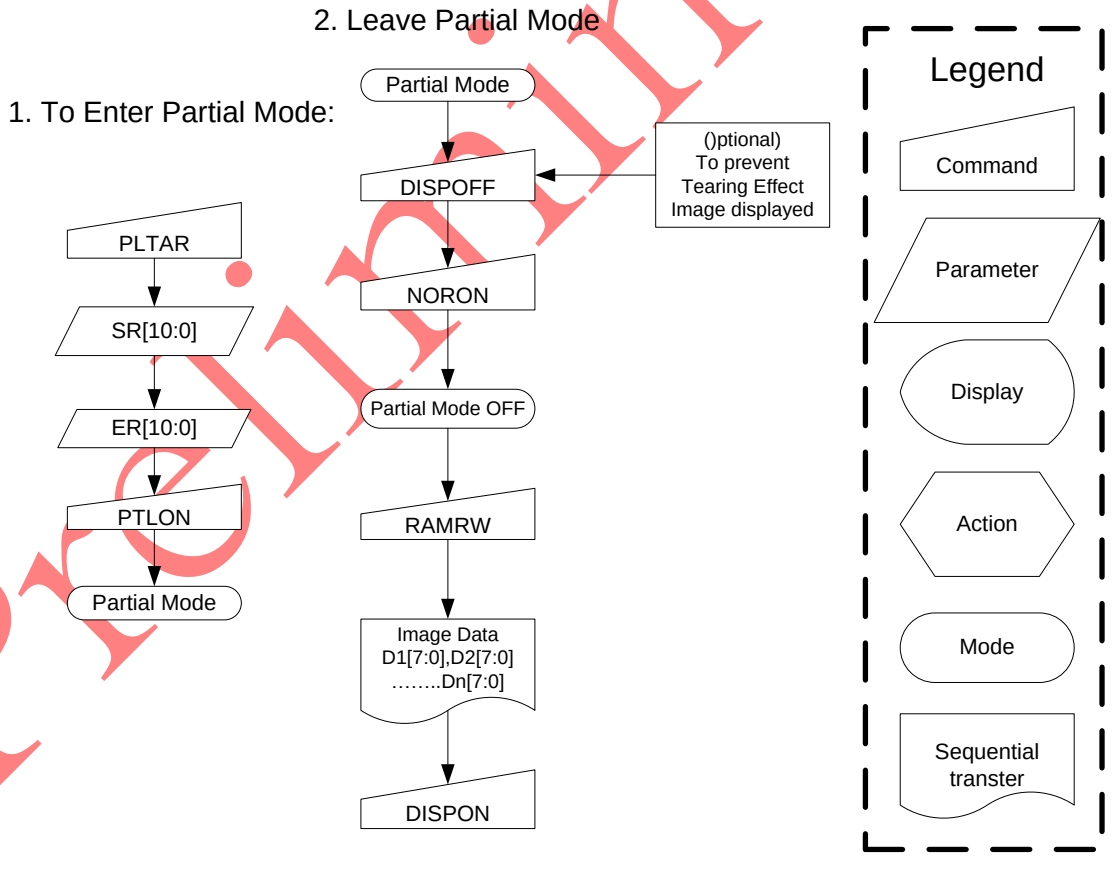
Restriction	Each detail initial value by the display resolution will be updated.
Register availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	SR[10:0]=0000h, ER=018Fh
S/W Reset	SR[10:0]=0000h, ER=018Fh
H/W Reset	SR[10:0]=0000h, ER=018Fh

Flow Chart



VSCRDEF (33h): Vertical Scrolling Definition

33H	VSCRDEF (Vertical Scrolling Definition)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VSCRDEF	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)

1st parameter	1	↑	1	-	-	-	-	-	-	TFA[10:8]	
2nd parameter	1	↑	1	-	TFA[7:0]						
3rd parameter	1	↑	1	-	-	-	-	-	-	VSA[10:8]	
4th parameter	1	↑	1	-	VSA[7:0]						
5th parameter	1	↑	1		-	-	-	-	-	BFA[10:8]	
6th parameter	1	↑	1		BFA[7:0]						

Description

-This command just defines the Vertical Scrolling Area of the display and not performs vertical scroll

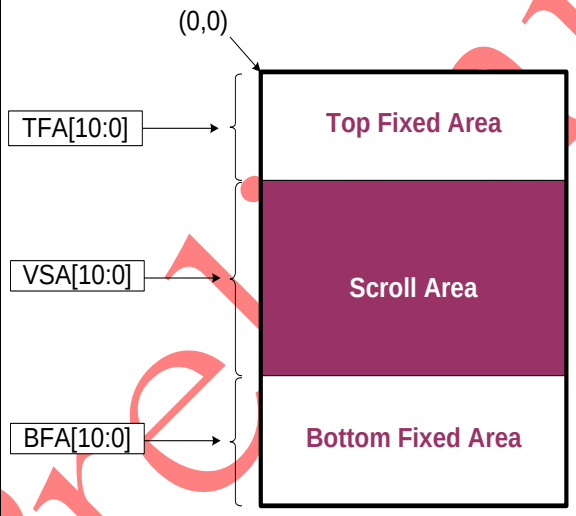
-When MADCTL MV=0

-The 1st & 2nd parameter TFA [10:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

-The 3rd & 4th parameter VSA [10:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address) The first line appears immediately after the bottom most line of the Top Fixed Area.

-The 4th & 5th parameter BFA [10:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

TFA, VSA and BFA refer to the Frame Memory Line Pointer



Restriction

The condition is TFA+VSA+BFA = YS[10:0]+YE[10:0], otherwise Scrolling mode is undefined.

In Vertical Scrolling Mode, MADCTL parameter MV should be set to '0' – this only affects the Frame Memory write.

Register availability

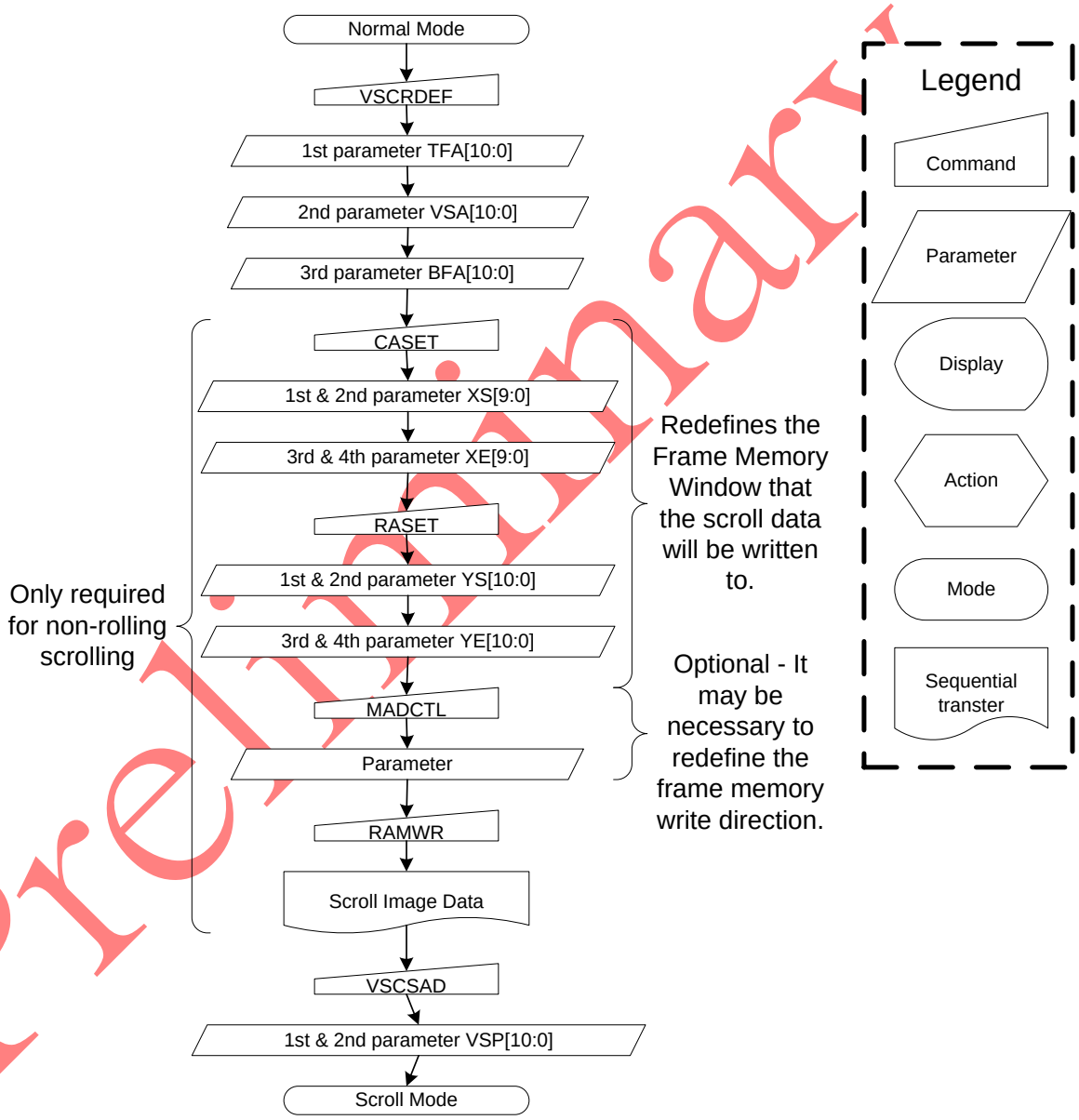
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
Power On Sequence	TFA[10:0] = 0000h	VSA[10:0] = 0000h	BFA[10:0] = 0000h
S/W Reset	TFA[10:0] = 0000h	VSA[10:0] = 0000h	BFA[10:0] = 0000h
H/W Reset	TFA[10:0] = 0000h	VSA[10:0] = 0000h	BFA[10:0] = 0000h

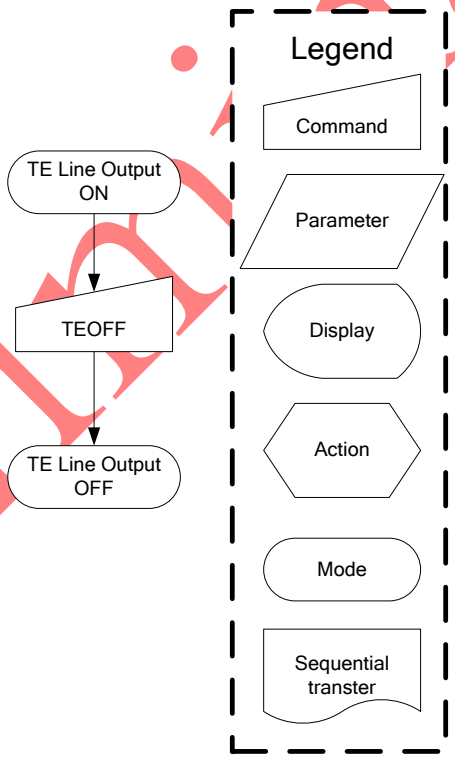
Flow Chart

1. TO Enter Vertical Scroll Mode:



TEOFF (34h): Tearing Effect Line OFF

34H	TEOFF (Tearing Effect Line OFF)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)

<table>
<tr><td>parameter</td><td>No Parameter</td></tr>
<tr><td>Description</td><td>-This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.</td></tr>
<tr><td>Restriction</td><td>This command has no effect when tearing effect output is already off..</td></tr>
<tr><td>Register availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Off</td></tr>
<tr><td>S/W Reset</td><td>Off</td></tr>
<tr><td>H/W Reset</td><td>Off</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

TEON (35h): Tearing Effect Line On

35H	TEON (Tearing Effect Line On)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)
parameter	1	↑	1	-	0	0	0	0	0	0	0	TE_MD	-

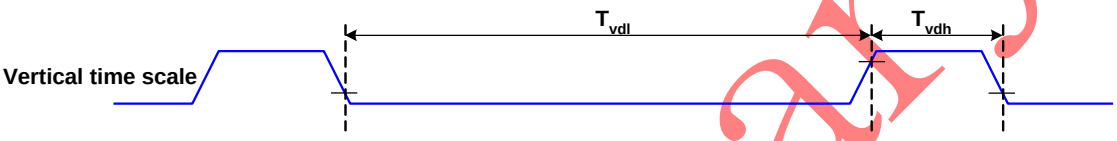
Description

-This command is used to turn ON the Tearing Effect output signal from the TE signal line.

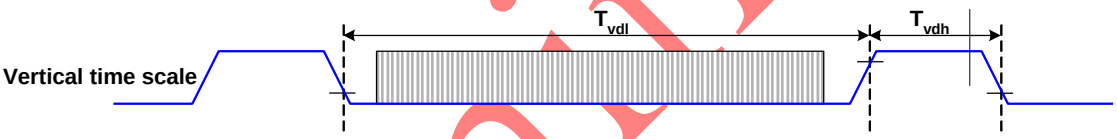
-This output is not affected by changing MADCTL bit ML.

-The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line:

-When TEM ='0': The Tearing Effect output line consists of V-Blanking information only



-When TEM ='1': The Tearing Effect output Line consists of both V-Blanking and H-Blanking information



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

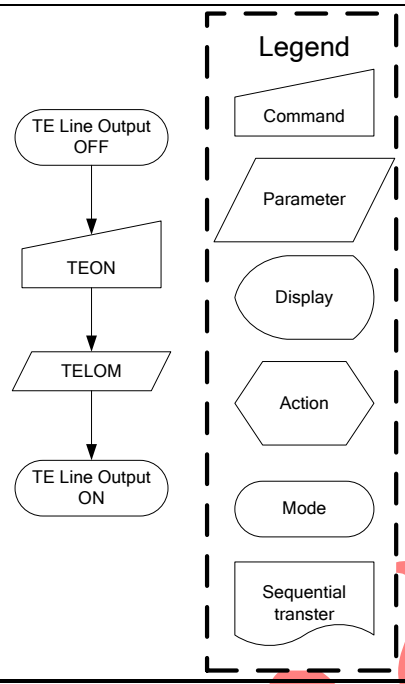
This command has no effect when tearing effect output is already on.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart	

MADCTL (36h): Memory Data Access Control

36H	MADCTL (Memory Data Access Control)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)
parameter	1	↑	1	-	MY	MX	-	ML	RGB	MH	-	-	

Description

-This command defines read/ write scanning direction of frame memory.

Bit	NAME	DESCRIPTION
D7	MY	Page Address Order
D6	MX	Column Address Order
D4	ML	Line Address Order
D3	RGB	RGB/BGR Order
D2	MH	Display Data Latch Order

-Bit Assignment

Bit D7- Page Address Order

"0" = Top to Bottom (When MADCTL D7="0").

"1" = Bottom to Top (When MADCTL D7="1").

Bit D6- Column Address Order

"0" = Left to Right (When MADCTL D6="0").

"1" = Right to Left (When MADCTL D6="1").

Bit D4- Line Address Order

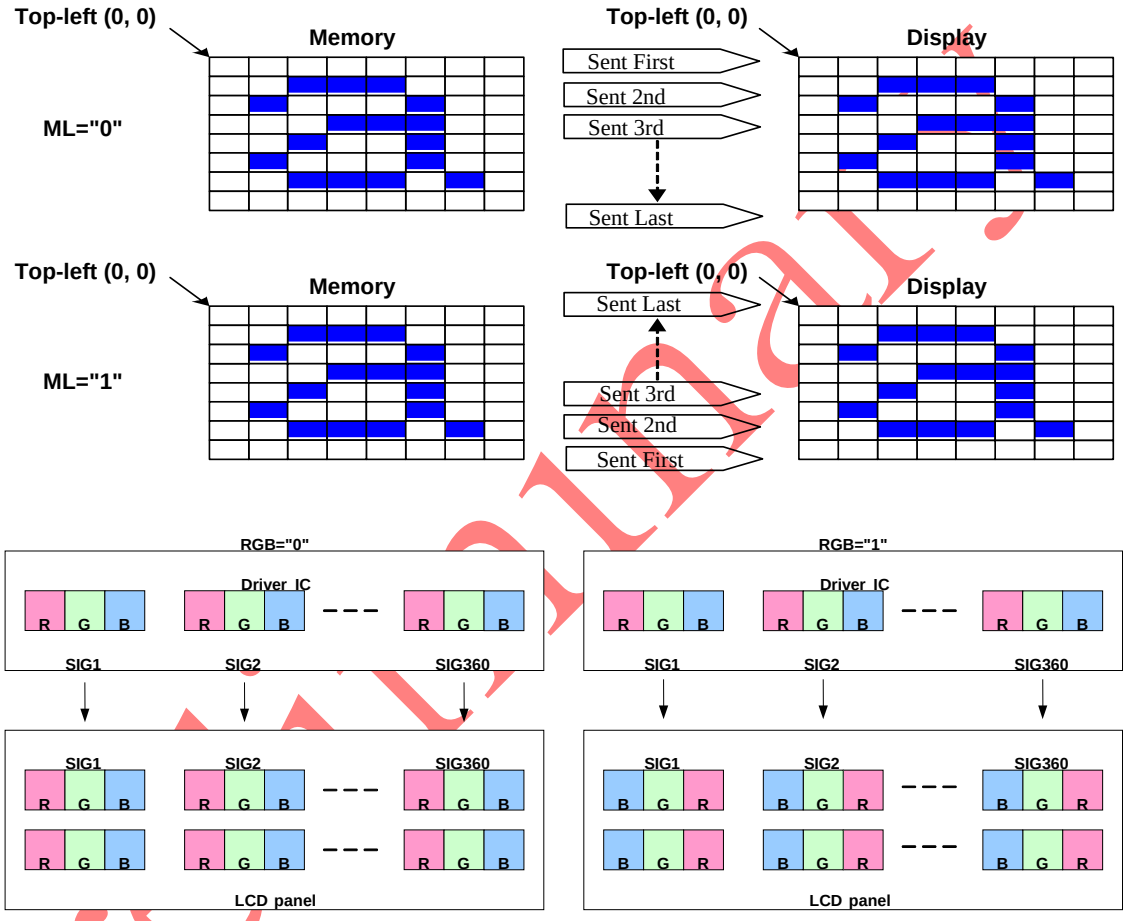
"0" = LCD Refresh Top to Bottom (When MADCTL D4="0")

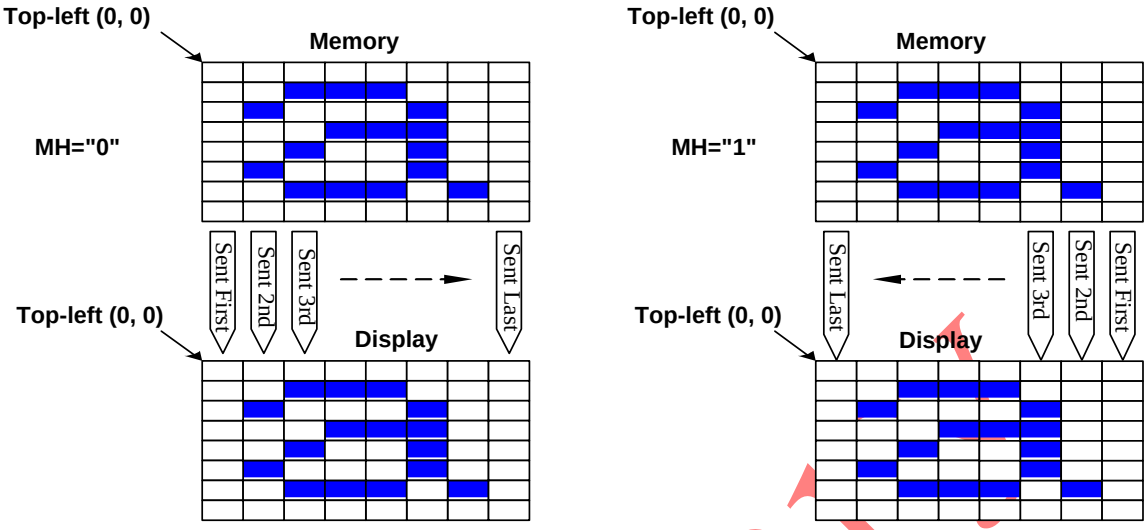
"1" = LCD Refresh Bottom to Top (When MADCTL D4="1")

Bit D3- RGB/BGR Order

“0” = RGB (When MADCTL D3=”0”)

“1” = BGR (When MADCTL D3=”1”)



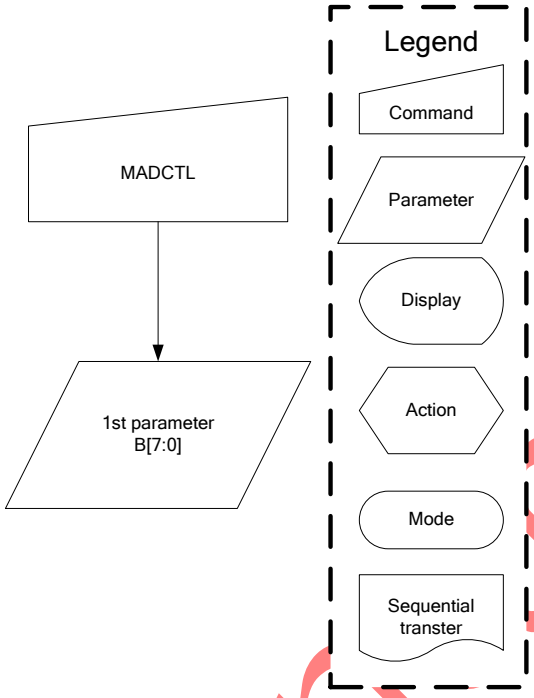


Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	No change
H/W Reset	0000h

Flow Chart	

VSCSAD (37h): Vertical Scroll Start Address of RAM

37H	VSCSAD (Vertical Scroll Start Address of RAM)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VSCSAD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)
1ST parameter	1	↑	1	-	-	-	-	-	-	VSP[10:8]			
2ND parameter	1	↑	1	VSP[7:0]									

Description

-This command is used together with Vertical Scrolling Definition (33h).

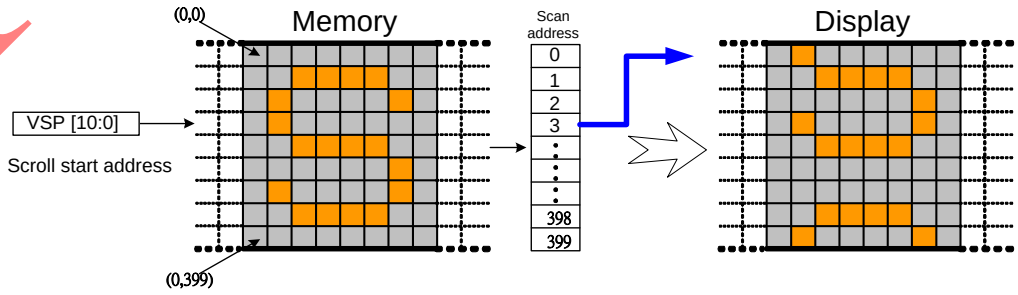
-These two commands describe the scrolling area and the scrolling mode.

-The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

When ML=0

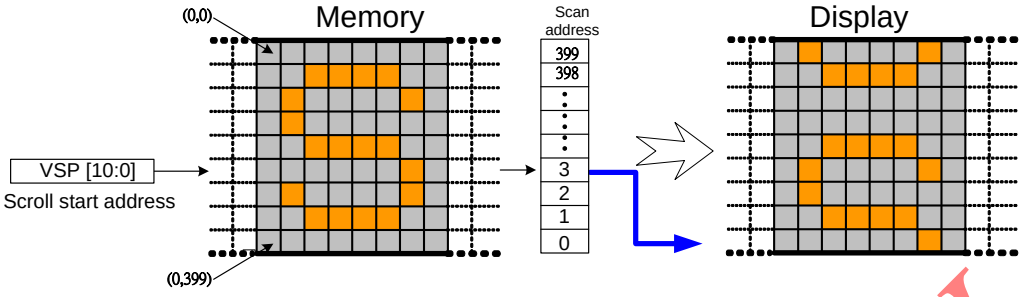
Example:

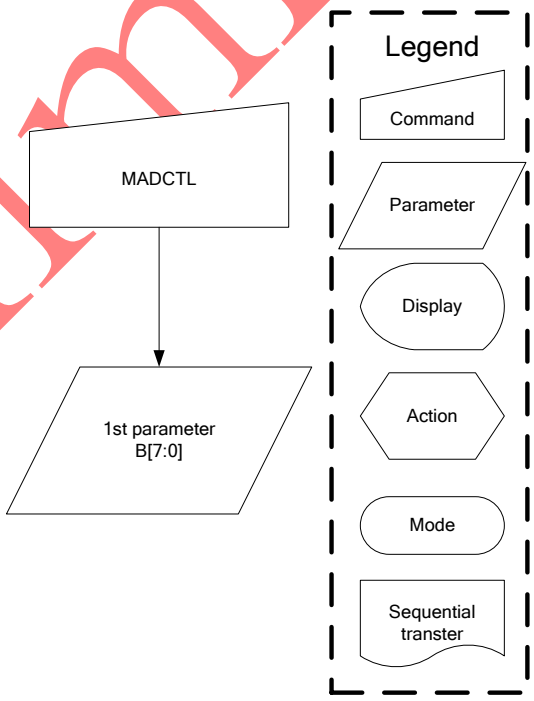
When Top Fixed Area = Bottom Fixed Area = 00, vertical Scrolling Area = 390 and VSP = '3'



When ML=1

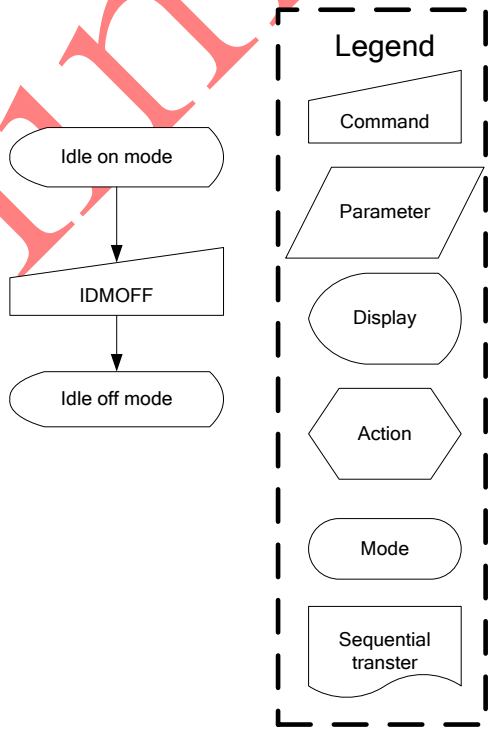
Example:

<table>
<tr><td></td><td>When Top Fixed Area = Bottom Fixed Area = 00, vertical Scrolling Area = 400 and VSP = ‘3’
 

NOTE: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.
VSP refers to the Frame Memory line Pointer</td></tr>
<tr><td>Register availability</td><td>Since the value of the vertical scrolling start address is absolute (with reference to the frame memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)- otherwise undesirable image will be displayed on the panel)</td></tr>
<tr><td>Default</td><td><table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0000h</td></tr>
<tr><td>S/W Reset</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td>0000h</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

IDMOFF (38h): Idle Mode Off

38H	IDMOFF (Idle Mode Off)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)

<table>
<tr><td>parameter</td><td>No Parameter</td></tr>
<tr><td>Description</td><td>-This command is used to recover from Idle mode on.
-In the idle off mode,
1. LCD can display 65k ,262k or 16.7m colors.
2. Normal frame frequency is applied.</td></tr>
<tr><td>Restriction</td><td>This command has no effect when module is already in idle off mode</td></tr>
<tr><td>Register availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Idle mode off</td></tr>
<tr><td>S/W Reset</td><td>Idle mode off</td></tr>
<tr><td>H/W Reset</td><td>Idle mode off</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

IDMON (39h): Idle Mode On

39H	IDMON (Idle Mode On)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)
parameter	No Parameter												

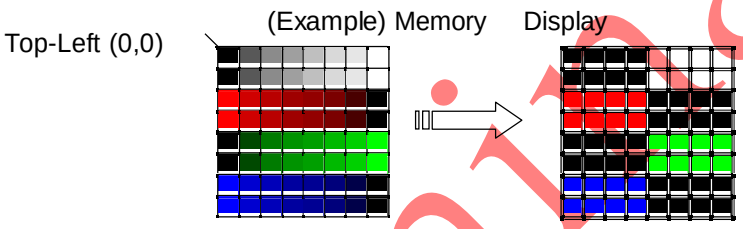
Description

-This command is used to enter into Idle mode on.

-There will be no abnormal visible effect on the display mode change transition.

-In the idle on mode,

1. Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from IDMON by Idle Mode Off (38h) command



Color	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B4 B1 B0
Black	0xxxxx	0xxxxx	0xxxxx
Blue	0xxxxx	0xxxxx	1xxxxx
Red	1xxxxx	0xxxxx	0xxxxx
Magenta	1xxxxx	0xxxxx	1xxxxx
Green	0xxxxx	1xxxxx	0xxxxx
Cyan	0xxxxx	1xxxxx	1xxxxx
Yellow	1xxxxx	1xxxxx	0xxxxx
White	1xxxxx	1xxxxx	1xxxxx

Restriction: This command has no effect when module is already in idle off mode

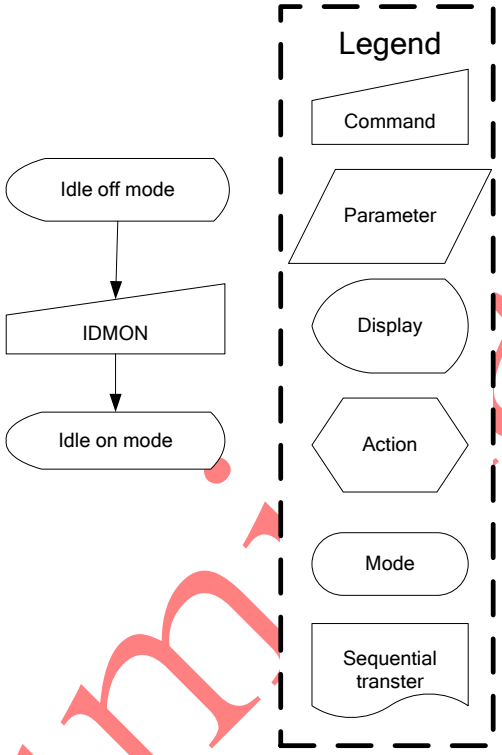
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	Idle mode off
S/W Reset	Idle mode off
H/W Reset	Idle mode off

Flow Chart



COLMOD (3Ah): Interface Pixel Format

3AH	COLMOD (Interface Pixel Format)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)
Parameter	1	↑	1	-	-	-			-	-	IFPF[1:0]		

Description

This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface. The formats are shown in the table:

1st parameter:

Bit	Name	Description
IFPF[1:0]	Control interface color format	'01' = 16bit/pixel '10' = 18bit/pixel '11' = 24bit/pixel

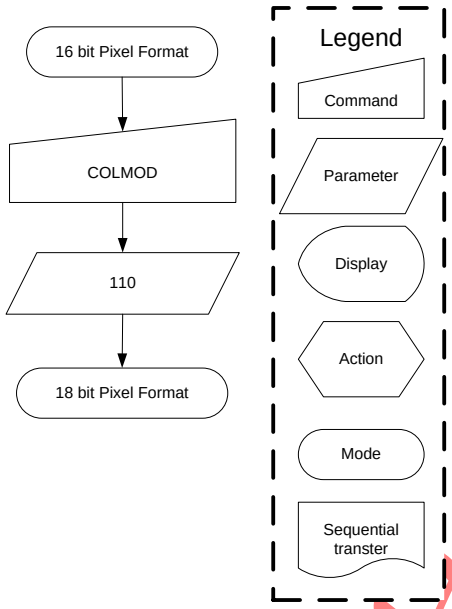
Note1: In 16-bit/Pixel,18-bit/Pixel,24-bit/Pixel mode, the LUT is applied to transfer data into the Frame Memory.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

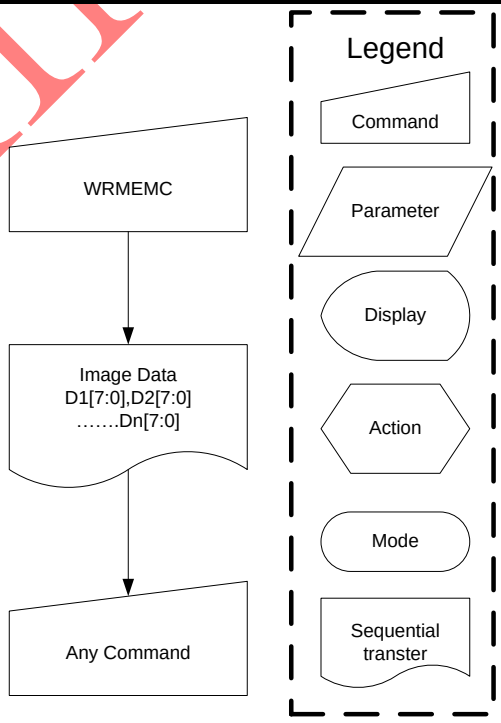
Default

Status	Default Value
Power On Sequence	24bit/pixel
S/W Reset	No change
H/W Reset	24bit/pixel

Flow Chart	

WRMEMC (3Ch): Write Memory Continue

3CH	WRMEMC (Write Memory Continue)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRMEMC	0	↑	1	-	0	0	1	0	1	1	0	0	(3Ch)
1ST parameter	1	↑	1	-	D1[7:0]								-
⋮	1	↑	1	-	Dx[7:0]								-
Nth parameter	1	↑	1	-	Dn[7:0]								-
Description	-This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write memory continue or memory write command. -If MV=0: Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the end column (XE) value. The column register is then reset to XS and the page register is incremented. Pixels are written to the frame memory until the page register equals the end page (YE) value and the column register equals the XE value, or the host processor sends another command. If the number of pixels exceeds (XE-XS+1)*(YE-YS+1) the extra pixels are ignored. If MV=1: Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the end page (YE) value. The page register is then reset to YS and the column register is incremented. Pixels are written to the frame memory until the column register equals the end column (XE) value and the page register equals the YE value, or the host processor sends another command. If the number of pixels exceeds (XE-XS+1)*(YE-YS+1) the extra pixels are ignored.												

	<table><tr><th>Condition</th><th>Column</th><th>Page</th></tr><tr><td>Command 2C is accepted</td><td>Return to “Start Column”</td><td>Return to “Start Page”</td></tr><tr><td>Read/Write RAM action</td><td>Increment by 1</td><td>No change</td></tr><tr><td>Column value is large than “End Column”</td><td>Return to “Start Column”</td><td>Increment by 1</td></tr><tr><td>Page value is large than “End Page”</td><td>Return to “Start Column”</td><td>Return to “Start Page”</td></tr></table>
Restriction	A memory write should follow a column address set or page address set to define the write address. Otherwise, data written with write memory continue is written to undefined addresses.
Register availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>S/W Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>H/W Reset</td><td>Contents of memory is not cleared</td></tr></table>
Flow Chart	

RDMEMC (3Eh): Read Memory Continue

3EH	RDMEMC (Read Memory Continue)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDMEMC	0	↑	1	-	0	0	1	1	1	1	1	0	(3Eh)
1ST parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D1[7:0]								-
⋮	1	1	↑		Dx[7:0]								
(N+1)th parameter	1	1	↑	-	Dn[7:0]								-

Description

-This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous read memory continue or memory read command.

-If MV=0:

Pixels are read continuing from the pixel location after the read range of the previous memory read or read memory continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the end column (XE) value. The column register is then reset to XS and the page register is incremented. Pixels are read from the frame memory until the page register equals the end page (YE) value and the column register equals the XE value, or the host processor sends another command.

If MV=1:

Pixels are read continuing from the pixel location after the read range of the previous memory read or read memory continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the end page (YE) value. The page register is then reset to YS and the column register is incremented. Pixels are read from the frame memory until the column register equals the end column (XE) value and the page register equals the YE value, or the host processor sends another command

Restriction

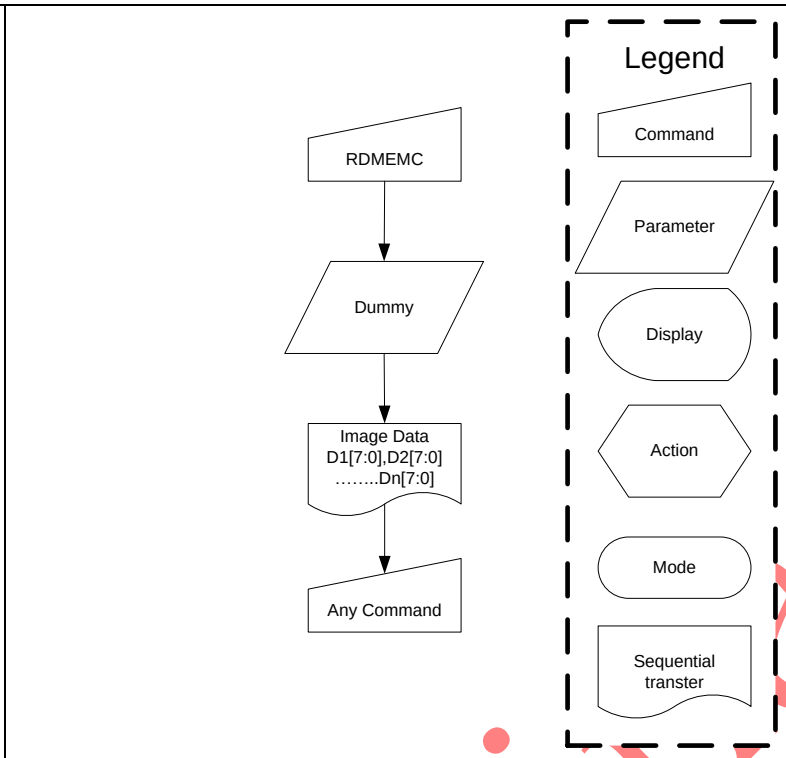
Regardless of the color mode set in interface pixel format, the pixel format returned by read memory continue is always 18-bit so there is no restriction on the length of data

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart	

SPIRDMD (42h): SPI Read Mode

42H	SPIRDMD (SPI Read Mode)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
COLMOD	0	↑	1	-	0	1	0	0	0	0	1	0	(42h)
Parameter	1	↑	1	-	SPI_RD_CAP[7:0]								
Description	- This command for SPI Read Mode. IF SPI Read ,SPI_RD_CAP[7:0]=0x5A												

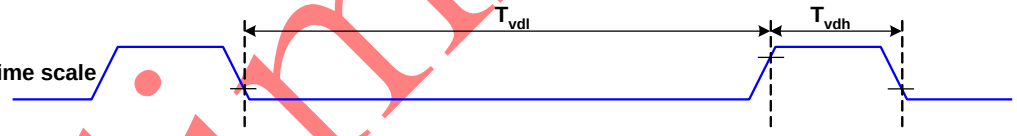
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

TESLWR (44h): Write Tear Scanline

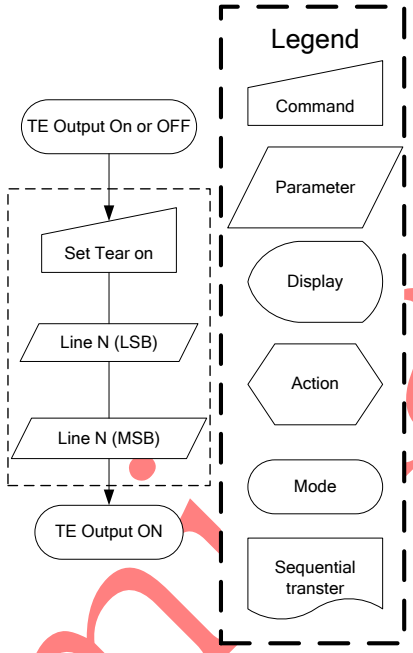
44H	STE (Write Tear Scanline)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TESLWR	0	↑	1	-	0	1	0	0	0	1	0	0	(44h)
1st parameter	1	↑	1	-	-	-	-	-	TE_SL[11:8]				
2nd parameter	1	↑	1	-	TE_SL[7:0]								
Description	-This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing MV. -The tearing effect line on has one parameter that describes the tearing effect output line mode. -The tearing effect output line consist of V-blanking information only. **Vertical time scale**  Note that set tear scanline with N=0 is equivalent to tearing effect line on with TEM=0. The tearing effect output line shall be active low when the display module is in sleep mode												
Restriction	This command takes effect on the frame following the current frame. Therefore, if the tear effect (TE) output is already on, the TE output shall continue to operate as programmed by the previous tearing effect line on or set tear scanline command until the end of the frame												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	
Flow Chart	

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h



TESLRD (45h): Read Tear Scanline

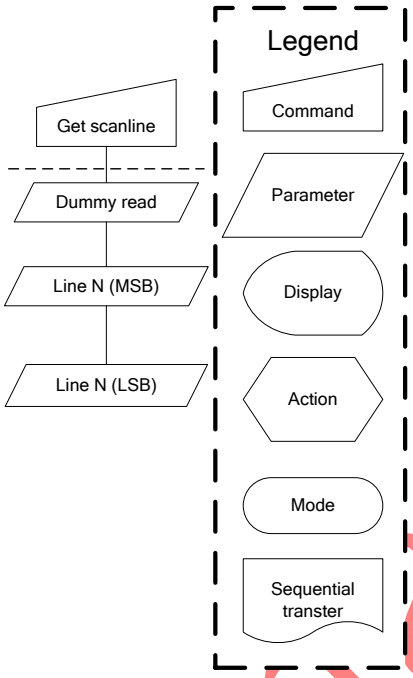
45H	TESLRD (Read Tear Scanline)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TESLRD	0	↑	1	-	0	1	0	0	0	1	0	1	(45h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	-	-	-	-	TE_SL[11:8]				
3rd parameter	1	1	↑	-	TE_SL[7:0]								
Description	-The display module returns the current scanline ,N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC+VBP+VACT+VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0. -When in sleep in mode, the value returned by get scanline is undefined. Note: that Set Tear Scan Line with N = 0 is equivalent to Tearing Effect Line ON with M = 0.												
Restriction	-												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart	

RAMCLACT (4Ch): Memory Clear Act

4CH	RAMCLACT (Memory Clear Act)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMCLACT	0	↑	1	-	0	1	0	0	1	1	0	0	(4Ch)
parameter	No Parameter												
Description	-This command is fill all pixels data in RAM.												
Restriction													

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart

RAMCLSET (4Dh): Memory Clear Setting

4DH	RAMCLSET (Memory Clear Setting)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMCLSETR	0	↑	1	-	0	1	0	0	1	1	0	1	(4Dh)
1st parameter	1	↑	1	-	CLNRAM_R[7:0]								
2nd parameter	1	↑	1	-	CLNRAM_G[7:0]								
3rd parameter	1	↑	1	-	CLNRAM_B[7:0]								
Description	CLNRAM_R/G/B[7:0]: Red/Green/Blue subpixel data setting when using RAMCLRACT(0x4Ch) function												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	000000h
S/W Reset	000000h
H/W Reset	000000h

RAMCLRBUSY (4Eh): Memory Clear Busy

45H	RAMCLRBUSY (Memory Clear Busy)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TESLRD	0	↑	1	-	0	1	0	0	1	1	1	0	(4Eh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	CLR_BUSY	
Description	- CLR_BUSY : Display memory is inoperable due to memory clear action												
Restriction	-												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes

	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

DTSB (4Fh): Deep Standby Mode on

4FH	DTSB (Deep Standby Mode on)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CDCCTR	0	↑	1	-	0	1	0	0	1	1	1	1	(4Fh)
1st parameter	1	↑	1	-	-	-	-	-	-	-	-	DSTB	
Description	-When DSTB =1 : Deep standby Mode ON Exit deep standby mode by pulling low “RESX” pin at least 1ms												
Restriction	-Only effect at Sleep in mpde												

Register availability

Status	Availability
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

WRDISBV (51h): Write Display Brightness

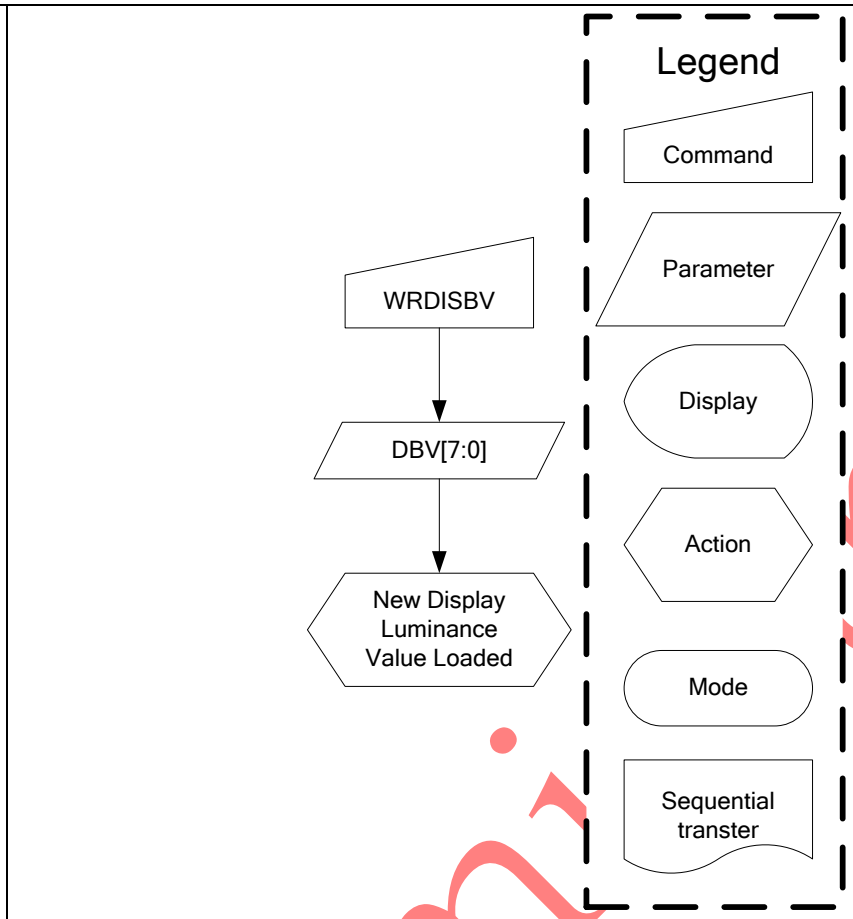
51H	WRDISBV (Write Display Brightness)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRDISBV	0	↑	1	-	0	1	0	1	0	0	0	1	(51h)
Parameter	1	↑	1	-	DBV[7:0]								
Description	-This command is used to adjust the brightness value of the display. -It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification. -In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.												
Restriction													

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart	

RDDISBV (52h): Read Display Brightness

52H	RDDISBV (Read Display Brightness Value)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDISBV	0	↑	1	-	0	1	0	1	0	0	1	0	(52h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	DBV[7:0]								(00h)
Description	-This command returns the brightness value of the display. -It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification is. -In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. -DBV[7:0] is reset when display is in sleep in mode. -DBV[7:0] is '0' when bit BCTRL of write CTRL display command (53h) is '0' -DBV[7:0] IS manual set brightness specified with write CTRL display command (53h) when bit BCTRL is '1'												
Restriction	-												
Register availability													

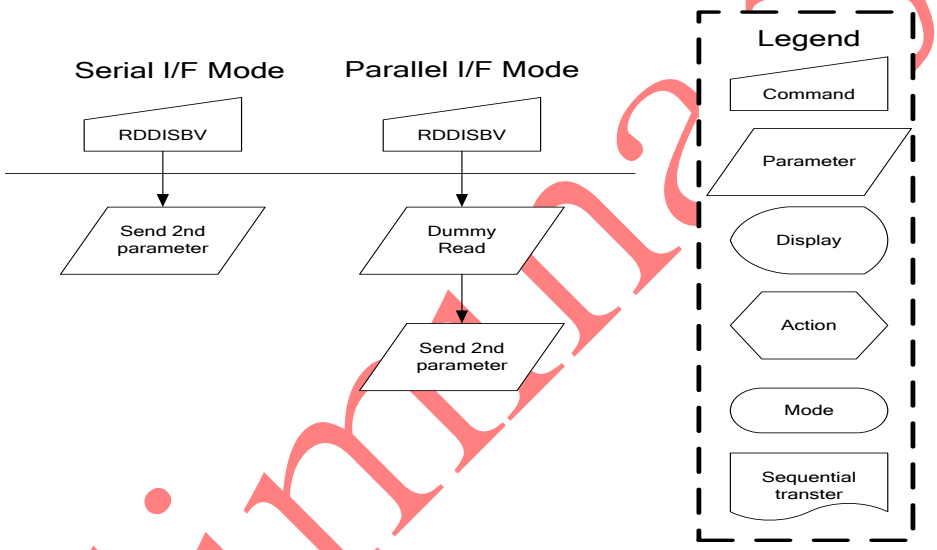
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes

Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart



WRCTRLD (53h): Write CTRL Display

53H	WRCTRLD (Write CTRL Display)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCTRLD	0	↑	1	-	0	1	0	1	0	0	1	1	(53h)
Parameter	1	↑	1	-	-	-	-	-	-	BL	-	-	-

Description

-This command is used to control display brightness.

-BL: Backlight Control On/Off

0 = Off (Completely turn off backlight circuit. Control lines must be low.)

1 = On

Restriction

Register availability

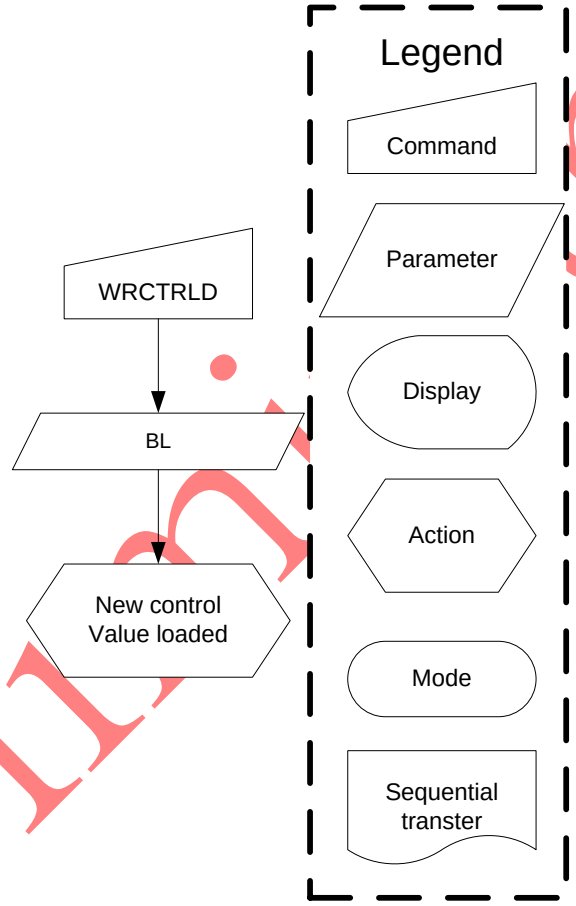
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes

Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

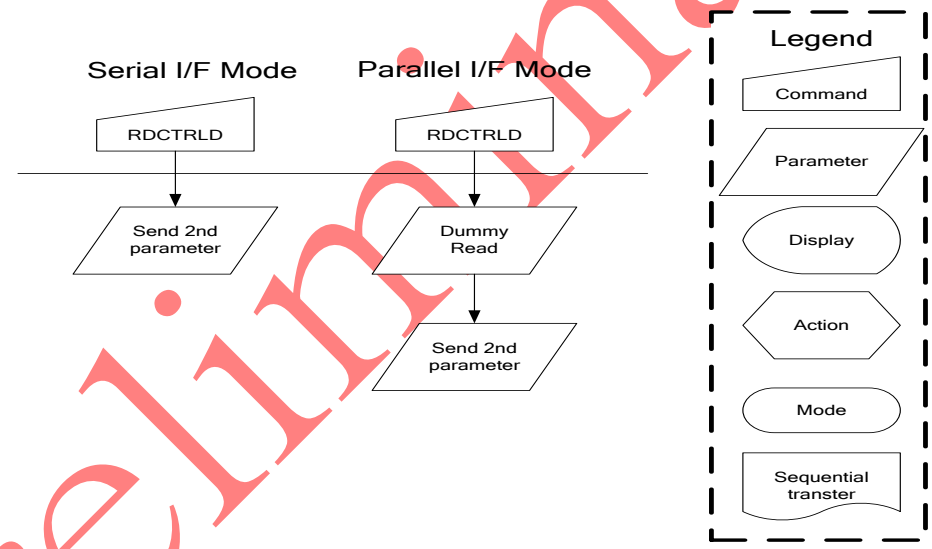
Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDCTRLD (54h): Read CTRL Display

54H	RDCTRLD (Read CTRL value Display)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCTRLD	0	↑	1	-	0	1	0	1	0	1	0	0	(54h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	-	-	-	-	-	BL	-	-	
Description	-This command returns ambient light and brightness control values. -BL: Backlight Control On/Off 0 = Off 1 = On												

Restriction	-
Register availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>
Flow Chart	

WRSRECTRL (55h): Write Content Adaptive Brightness Control

55H	WRSRECTRL (Write Content Adaptive Brightness Control)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCTRLD	0	↑	1	-	0	1	0	1	0	1	0	1	(55h)
Parameter	1	↑	1	-	-	SRE	-	-	-	-	-	-	
Description	-This command is used to control SRE. -SRE: CABC Sunlight Readable Enhance function enable 0 = Off 1 = On												
Restriction													

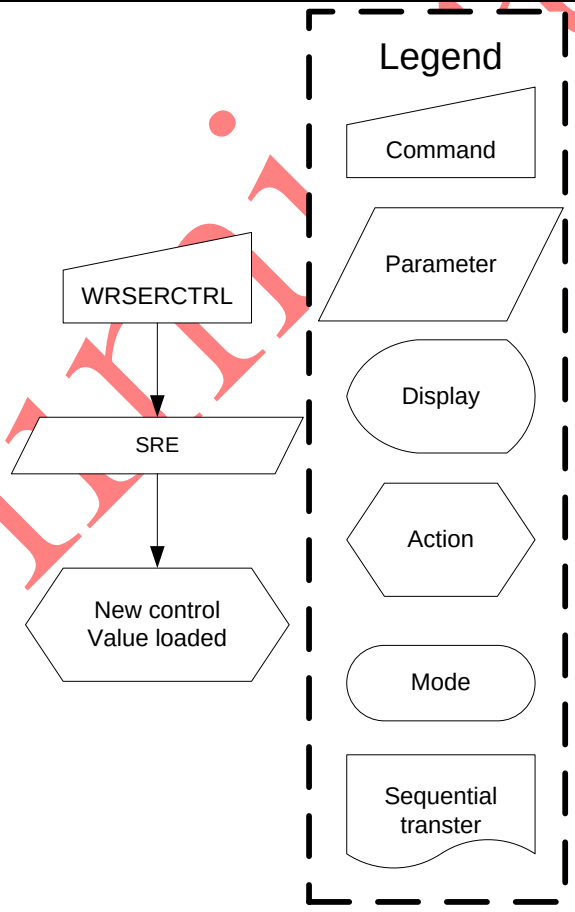
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDSRECTRL (56h): Read Content Adaptive Brightness Control

56H	RDSRECTRL (Read Content Adaptive Brightness Control)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCTRLD	0	↑	1	-	0	1	0	1	0	1	1	0	(56h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	

2nd parameter	1	1	↑	-	-	SRE	-	-	-	-	-	-	

Description	-This command returns SRE Status -SRE: CABC Sunlight Readable Enhance function enable 0 = Off 1 = On
Restriction	-

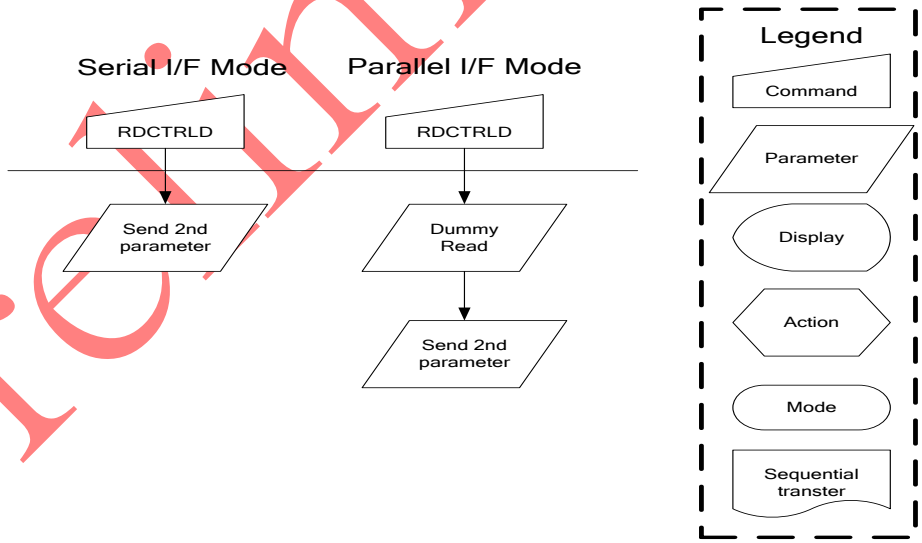
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDFCS (AAh): Read First Checksum

AAH	RDFCS (Read First Checksum)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCTRLD	0	↑	1	-	1	0	1	0	1	0	1	0	(AAh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	FCS[7:0]								

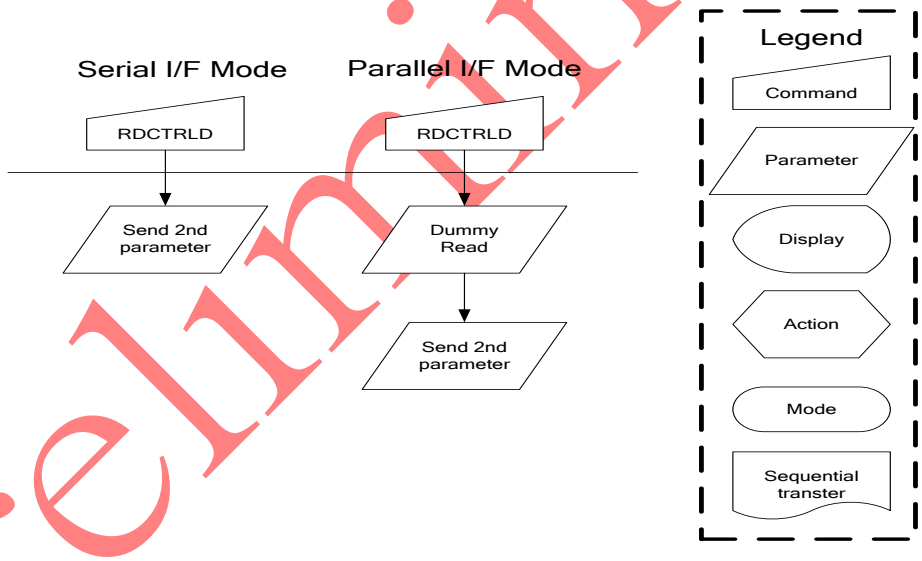
Description	-Read the first checksum that has been calculated from user commands after write access to these commands has been done.
Restriction	-only in sleep out mode
Register availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDCCS (AFh): Read Continue Checksum

AFH	RDCCS (Read Continue Checksum)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCTRLD	0	↑	1	-	1	0	1	0	1	1	1	1	(AFh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	FCS[7:0]								
Description	- Read the continue checksum that has been calculated continuously after the first checksum has calculated from user commands after write access to these commands has been done.												
Restriction	-only in sleep out mode												
Register													

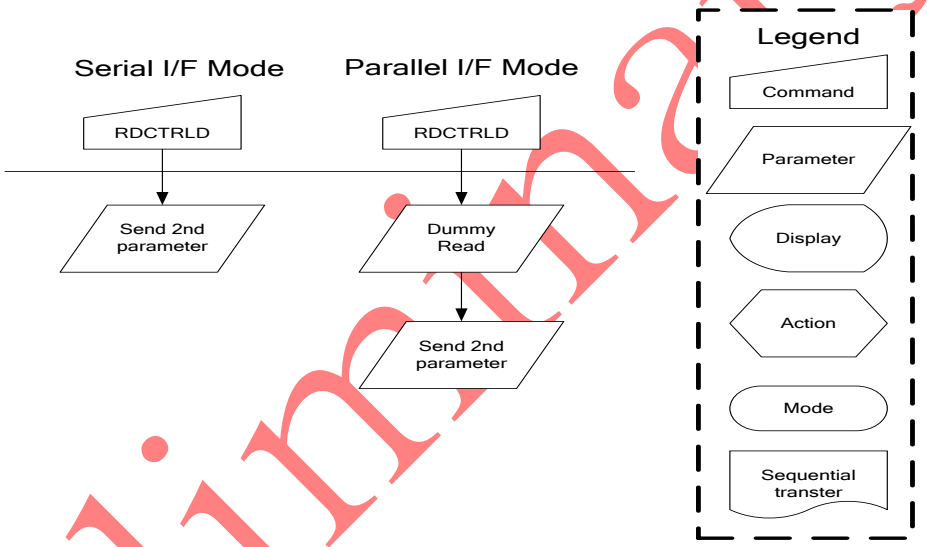
availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RAMMD (D0h): RAM Mode

D0H	RAMMD (RAM Mode)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCTRLD	0	↑	1	-	1	1	0	1	0	0	0	0	(D0h)
Parameter	1	↑	1	-	scan_ ram_spwr	-	-	-	-	-	Video_mode [1:0]		
Description	-Video_mode[1:0]: 0 = with RAM Compression On Ex. Resolution 400x400 2 = with RAM Compression Off Ex. Resolution 200x400 3 = without RAM Ex. Resolution 560x640												
Restriction													

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	81h
S/W Reset	81h
H/W Reset	81h

RDID1 (DAh): Read ID1

DAH	RDID1 (Read ID1)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)
1st parameter	1	1	↑	-	-								
2nd parameter	1	1	↑	-	ID1[7:0]								
Description	-This read byte identifies the LCD module's manufacturer. '-': Don't care.												

Register availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

RDID2 (DBh): Read ID2

DBH	RDID2 (Read ID2)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)
1st parameter	1	1	↑	-	-								
2nd parameter	1	1	↑	-	ID2[7:0]								
Description	This read byte is used to track the LCD module/driver IC version. '-': Don't care.												

Register availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

RDID3 (DCh): Read ID3

DCH	RDID3 (Read ID3)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)
1st parameter	1	1	↑	-	-								
2nd parameter	1	1	↑	-	ID3[7:0]								
Description	This read byte identifies the LCD module/driver. '-': Don't care.												
Register availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

13.3 Command Table 2

COMMAND Table 2														
Instruction	**D/CX**	**WRX**	**RDX**	**PNUM**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
PWMCTRL	0	↑	1	3	0	1	1	0	0	0	0	0	(60h)	PWM Control
	1	↑	1		-	0	0	0	-	0	0	0		
	1	↑	1		-	-	PWM_CLK_SEL[5:0]							
	1	↑	1		-	-	-	-	0	0	0	0		
LBCTRL	0	↑	1	1	0	1	1	0	0	1	1	0	(66h)	Line Buffer Control
	1	↑	1		-	-	-	-	-	-	SSI	-		
TIMCTRL	0	↑	1	12	0	1	1	1	0	0	0	0	(70h)	TIMING CTRL
	1	↑	1		-	-	-	-	-	-	RTN[9:8]			
	1	↑	1		RTN[7:0]									
	1	↑	1		-	Y_Res[10:8]			-	-	X_Res[9:8]			
	1	↑	1		X_Res[7:0]									
	1	↑	1		Y_Res[7:0]									
	1	↑	1		-	-	-	VBP[8]	-	-	VFP[9:8]			
	1	↑	1		VBP[7:0]									
	1	↑	1		VFP[7:0]									
	1	↑	1		-	-	0	0	-	-	0	0		
	1	↑	1		0	0	0	0	0	0	0	0		
	1	↑	1		-	-	-	-	-	-	0	0		
	1	↑	1		0	0	0	1	1	0	1	0		
DISPMODE	0	↑	1	1	0	1	1	1	0	0	0	1	(71h)	Display Mode
	1	↑	1		1	1	Nline[1:0]		0	-	Hsync_sel	Disp_ mode		
NVMID	0	↑	1	3	1	0	1	1	0	0	0	1	(B1h)	NVM ID Setting
	1	↑	1		ID1_PROG_DATA[7:0]									
	1	↑	1		ID2_PROG_DATA[7:0]									
	1	↑	1		ID3_PROG_DATA[7:0]									
GAMCTRP	0	↑	1	16	1	0	1	1	0	1	1	1	(B7h)	GAMCTRP
	1	↑	1		-				VC0P[3:0]					
	1	↑	1		-	-	VC1P[5:0]							
	1	↑	1		-	-	VC2P[5:0]							
	1	↑	1		-	-	-	VC4P[4:0]						
	1	↑	1		-	-	-	VC6P[4:0]						

COMMAND Table 2														
Instruction	**D/CX**	**WRX**	**RDX**	**PNUM**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
	1	↑	1			-			VC13P[3:0]					
	1	↑	1		-	VC20P[6:0]								
	1	↑	1		-	-			-	VC27P[2:0]				
	1	↑	1			-				VC36P[2:0]				
	1	↑	1		-	VC43P[6:0]								
	1	↑	1		-	-			VC50P[3:0]					
	1	↑	1		-	-	-	VC57P[4:0]						
	1	↑	1		-	-	-	VC59P[4:0]						
	1	↑	1		-	-	VC61P[5:0]							
	1	↑	1		-	-	VC62P[5:0]							
	1	↑	1		-	-	-	-	VC63P[3:0]					
GAMCTRN	0	↑	1	16	1	0	1	1	1	0	0	0	(B8h)	GAMCTRN
	1	↑	1		-				VC0N[3:0]					
	1	↑	1		-	-	VC1N[5:0]							
	1	↑	1		-	-	VC2N[5:0]							
	1	↑	1		-	-	-	VC4N[4:0]						
	1	↑	1		-	-	-	VC6N[4:0]						
	1	↑	1		-	-	-	-	VC13N[3:0]					
	1	↑	1		-	VC20N[6:0]								
	1	↑	1		-	-	-	-	-	VC27N[2:0]				
	1	↑	1			-	-	-	-	VC36N[2:0]				
	1	↑	1		-	VC43N[6:0]								
	1	↑	1		-	-	-	-	VC50N[3:0]					
	1	↑	1		-	-	-	VC57N[4:0]						
	1	↑	1		-	-	-	VC59N[4:0]						
	1	↑	1		-	-	VC61N[5:0]							
	1	↑	1		-	-	VC62N[5:0]							
	1	↑	1		-	-	-	-	VC63N[3:0]					GAMCTR
GAMCTR	0	↑	1	2	1	0	1	1	1	0	0	0	(B9h)	
	1	↑	1		-	AJ0P[2:0]				AJ1P[2:0]				
	1	↑	1		-	AJ0N[2:0]				AJ1N[2:0]				
VCOM_SSI	0	↑	1	3	1	0	1	1	1	1	1	0	(BEh)	VCOM_SSI Control
	1	↑	1		-	VCMP[6:0]								
	1	↑	1		-	-	-	-	-	-	-	SSI_pos[8]		

COMMAND Table 2														
Instruction	**D/CX**	**WRX**	**RDX**	**PNUM**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
	1	↑	1		SSI_pos[7:0]									
VGH_VGL CTRL	0	↑	1	6	1	0	1	1	1	1	1	1	(BFh)	
	1	↑	1		-	-	-	VGHP_DISP[4:0]						
	1	↑	1		-	-	-	VGHP_TP[4:0]						
	1	↑	1		-	-	-	VGHP_NOISE[4:0]						
	1	↑	1		-	-	-	-	VGLS_DP[3:0]					
	1	↑	1		-	-	-	-	VGLS_TP[3:0]					
	1	↑	1		-	-	-	-						

PWMCTRL (60h): PWM control

60H	PWMCTRL(PWM control)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWMCTRL	0	↑	1	-	0	1	1	0	0	0	0	0	(60h)
1st Parameter	1	↑	1	-	-	0	0	0	-	0	0	0	
2nd Parameter	1	↑	1	-	-	-	PWM_CLK_SEL[5:0]						
3rd Parameter	1	↑	1	-	-	-	-	-	0	0	0	0	

Description

PWM_CLK_SEL[5:0]: PWM clock select

CK_SEL	PWM Frequency(KHz)	CK_SEL	PWM Frequency(KHz)	CK_SEL	PWM Frequency(KHz)	CK_SEL	PWM Frequency(KHz)
0	58.824	16	6.920	32	3.565	48	2.401
1	58.824	17	6.536	33	3.460	49	2.353
2	39.216	18	6.192	34	3.361	50	2.307
3	29.412	19	5.882	35	3.268	51	2.262
4	23.529	20	5.602	36	3.180	52	2.220
5	19.608	21	5.348	37	3.096	53	2.179
6	16.807	22	5.115	38	3.017	54	2.139
7	14.706	23	4.902	39	2.941	55	2.101
8	13.072	24	4.706	40	2.869	56	2.064
9	11.765	25	4.525	41	2.801	57	2.028
10	10.695	26	4.357	42	2.736	58	1.994
11	9.804	27	4.202	43	2.674	59	1.961
12	9.050	28	4.057	44	2.614	60	1.929
13	8.403	29	3.922	45	2.558	61	1.898
14	7.843	30	3.795	46	2.503	62	1.867
15	7.353	31	3.676	47	2.451	63	1.838

'-': Don't care

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h/00h/08h
S/W Reset	00h/00h/08h
H/W Reset	00h/00h/08h

LBCTRL (66h): Line Buffer control

66H	LBCCTRL(Line Buffer control)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
LBCTRL	0	↑	1	-	0	1	1	0	0	1	1	0	(66h)
1st Parameter	1	↑	1	-	-	-	-	-	-	-	SSI	-	
Description	**SSI:** For Source partial off function Resolution = 280 , this bit set to 0 Other resolution , this bit set to 1 & Set “CMD 0xBE ssi_en_start_pos[7:0]” ‘-’: Don’t care												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

TIMINGCTRL (70h): Timing control

70H	TIMINGCTRL(Timing control)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TIMINGCTRL	0	↑	1	-	1	1	1	0	0	0	0	0	(70h)
1st Parameter	1	↑	1	-	-	-	-	-	-	-	RTN[9:8]		
2nd Parameter	1	↑	1	-	RTN[7:0]								
3rd Parameter	1	↑	1	-	-	Y_Res[10:8]			-	-	X_Res[9:8]		
4th Parameter	1	↑	1	-	X_Res[7:0]								
5th Parameter	1	↑	1	-	Y_Res[7:0]								
6th Parameter	1	↑	1	-	-	-	-	VBP[8]	-	-	VFP[9:8]		
7th Parameter	1	↑	1	-	VBP[7:0]								
8th Parameter	1	↑	1	-	VFP[7:0]								
9th Parameter	1	↑	1	-	-	-	0	0	-	-	0	0	
10th Parameter	1	↑	1	-	0	0	0	0	0	0	0	0	
11th Parameter	1	↑	1	-	-	-	-	-	-	-	-	0	
12th Parameter	1	↑	1	-	0	0	0	1	1	0	1	0	

Description

RTN[9:0]: define frame rate. RTN min. = 2

$$\text{Frame Rate} = \frac{15{,}000{,}000}{(Y\_Res+VBP+VFP) \times RTN}$$

RTN[9:0]	FR(Hz)	RTN[9:0]	FR(Hz)	RTN[9:0]	FR(Hz)	RTN[9:0]	FR(Hz)
1BBh	70.84	251h	52.92	2E7h	42.24	37Dh	35.14
1C5h	69.27	25Bh	52.04	2F1h	41.67	387h	34.75
1CFh	67.78	265h	51.19	2FBh	41.13	391h	34.37
1D9h	66.34	26Fh	50.37	305h	40.60	39Bh	34.00
1E3h	64.97	279h	49.57	30Fh	40.08	3A5h	33.63
1Edh	63.65	283h	48.80	319h	39.57	3AFh	33.28
1F7h	62.39	28Dh	48.06	323h	39.08	3B9h	32.93
201h	61.17	297h	47.33	32Dh	38.60	3C3h	32.59
20Bh	60.00	2A1h	46.63	337h	38.13	3CDh	32.25
215h	58.88	2Abh	45.95	341h	37.67	3D7h	31.92
21Fh	57.79	2B5h	45.28	34Bh	37.23	3E1h	31.60
229h	56.75	2BFh	44.64	355h	36.79	3EBh	31.29
233h	55.74	2C9h	44.01	35Fh	36.36	3F5h	30.98
23Dh	54.77	2D3h	43.40	369h	35.95	3FFh	30.68
247h	53.83	2DDh	42.81	373h	35.54	-	

<table>
<tr><td></td><td>Note:
1. In this frame rate table , Y_Res = 400 , VFP = 60 , VBP = 18
2. The deviation of frame rate is +/- 5%
X_Res[9:0]: X resolution
Y_Res[10:0]: Y resolution
VBP[8:0]: Vertical back porch lines. VBP min =1
VFP[9:0]: Vertical front porch lines. VFP min =1
‘-’: Don’t care</td></tr>
<tr><td>Register Availability</td><td><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td><table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h/beh/51h/18h/00h/00h/04h/1ah/11h/33h/00h/3Fh</td></tr>
<tr><td>S/W Reset</td><td>00h/beh/51h/18h/00h/00h/04h/1ah/11h/33h/00h/3Fh</td></tr>
<tr><td>00h/beh/51h/18h/00h/00h/04h/1ah</td><td>00h/beh/51h/18h/00h/00h/04h/1ah/11h/33h/00h/3Fh</td></tr>
</table></td></tr>
</table>

DISPMODE (71h): Display mode

71H	DISPMODE(Display mode)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
LBCTRL	0	↑	1	-	0	1	1	1	0	0	0	1	(71h)
1st Parameter	1	↑	1	-	0	0	Nline[1:0]		0	-	Hsync_sel	Disp_mode	
Description	**Nline[1:0]:** For inversion in normal mode 0 = Column inversion , 1 = 1-Dot inversion , 2 = 2-Dot inversion **Hsync_sel:** 0 = internal h-sync , 1 = external h-sync (Valid @disp_mode=1) **Disp_mode:** 0 = internal mode , 1 = external mode (video with v-sync) '-': Don't care												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	C3h
S/W Reset	C3h
H/W Reset	C3h

NVMID (B1h): NVM ID Setting

B1H	NVMID(NVM ID Setting)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVMID	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)
1st Parameter	1	↑	1	-	ID1_PROG_DATA[7:0]								
2nd Parameter	1	↑	1	-	ID2_PROG_DATA[7:0]								
3rd Parameter	1	↑	1	-	ID3_PROG_DATA[7:0]								
Description	**ID1/2/3_PROG_DATA[7:0]:** For NVM ID Program '-': Don't care												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

GAMCTRP (B7h): Positive Voltage Gamma Control

B7H	GAMCTRP (Positive Voltage Gamma Control)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMCTRP1	0	↑	1	-	1	0	1	1	0	0	0	0	(B7h)
1st Parameter	1	↑	1	-	-	-	-	-	VC0P[3:0]				
2nd Parameter	1	↑	1	-	-	-	VC1P[5:0]						
3rd Parameter	1	↑	1	-	-	-	VC2P[5:0]						
4th Parameter	1	↑	1	-	-	-	-	VC4P[4:0]					
5th Parameter	1	↑	1	-	-	-	-	VC6P[4:0]					
6th Parameter	1	↑	1	-	-	-	-	-	VC13P[3:0]				
7th Parameter	1	↑	1	-	-	VC20P[6:0]							
8th Parameter	1	↑	1	-	-	-	-	-	-	VC27P[2:0]			
9th Parameter	1	↑	1	-	-	-	-	-	-	VC36P[2:0]			
10th Parameter	1	↑	1	-	-	VC43P[6:0]							
11th Parameter	1	↑	1	-	-	-	-	-	VC50P[3:0]				
12th Parameter	1	↑	1	-	-	-	-	VC57P[4:0]					
13th Parameter	1	↑	1	-	-	-	-	VC59P[4:0]					
14th Parameter	1	↑	1	-	-	-	VC61P[5:0]						
15th Parameter	1	↑	1	-	-	-	VC62P[5:0]						
16th Parameter	1	↑	1	-	-	-	-	-	VC63P[3:0]				

Description

Adjust the gamma characteristics of the TFT panel.

Positive Gamma Control

'-': Don't care

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Refer to description
S/W Reset	Refer to description
H/W Reset	Refer to description

GAMCTRN (B8h): Native Voltage Gamma Control

B8H	GAMCTRN (Native Voltage Gamma Control)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMCTRN	0	↑	1	-	1	0	1	1	1	0	0	0	(B8h)
1st Parameter	1	↑	1	-	-	-	-	-	VC0N[3:0]				
2nd Parameter	1	↑	1	-	-	-	VC1N[5:0]						
3rd Parameter	1	↑	1	-	-	-	VC2N[5:0]						
4th Parameter	1	↑	1	-	-	-	-	VC4N[4:0]					
5th Parameter	1	↑	1	-	-	-	-	VC6N[4:0]					
6th Parameter	1	↑	1	-	-	-	-	-	VC13N[3:0]				
7th Parameter	1	↑	1	-	-	VC20N[6:0]							
8th Parameter	1	↑	1	-	-	-	-	-	-	VC27N[2:0]			
9th Parameter	1	↑	1	-	-	-	-	-	-	VC36P[2:0]			
10th Parameter	1	↑	1	-	-	VC43P[6:0]							
11th Parameter	1	↑	1	-	-	-	-	-	VC50P[3:0]				
12th Parameter	1	↑	1	-	-	-	-	VC57P[4:0]					
13th Parameter	1	↑	1	-	-	-	-	VC59P[4:0]					
14th Parameter	1	↑	1	-	-	-	VC61P[5:0]						
15th Parameter	1	↑	1	-	-	-	VC62P[5:0]						
16th Parameter	1	↑	1	-	-	-	-	-	VC63P[3:0]				
Description	Adjust the gamma characteristics of the TFT panel. Native Gamma Control '-': Don't care												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Refer to description
S/W Reset	Refer to description
H/W Reset	Refer to description

GAMCTR (B9h): Gamma Control

B9H	GAMCTR (Gamma Control)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMCTRP1	0	↑	1	-	1	0	1	1	1	0	0	1	(B9h)
1st Parameter	1	↑	1	-	-	AJ0P[2:0]			-	AJ1P[2:0]			
2nd Parameter	1	↑	1	-	-	AJ0N[2:0]			-	AJ1N[2:0]			
Description	Adjust the gamma characteristics of the TFT panel. '-': Don't care												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Refer to description
S/W Reset	Refer to description
H/W Reset	Refer to description

VCOM_SSI CTRL (BEh): VCOM_SSI Control

BEH	VCOM_SSI CTRL (VCOM_SSI Control)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VCOM_SSI CTRL	0	↑	1	-	1	0	1	1	1	1	1	0	(BEh)
1st Parameter	1	↑	1	-	-	VCM[6:0]							
2nd Parameter	1	↑	1	-	-	-	-	-	-	-	-	SSI_pos[8]	
3rd Parameter	1	↑	1	-	SSI_pos[7:0]								

Description

VCM[6:0]: VCOMS Set.

VCM[6:0]	VCOMS (V)	VCM[6:0]	VCOMS (V)
00h	0.100	30h	1.300
01h	0.125	31h	1.325
02h	0.150	32h	1.350
03h	0.175	33h	1.375
04h	0.200	34h	1.400
05h	0.225	35h	1.425
06h	0.250	36h	1.450
07h	0.275	37h	1.475
08h	0.300	38h	1.500
09h	0.325	39h	1.525
0Ah	0.350	3Ah	1.550
0Bh	0.375	3Bh	1.575
0Ch	0.400	3Ch	1.600
0Dh	0.425	3Dh	1.625
0Eh	0.450	3Eh	1.650
0Fh	0.475	3Fh	1.675
10h	0.500	40h	1.700
11h	0.525	41h	1.725
12h	0.550	42h	1.750
13h	0.575	43h	1.775
14h	0.600	44h	1.800
15h	0.625	45h	1.825
16h	0.650	46h	1.850
17h	0.675	47h	1.875
18h	0.700	48h	1.900
19h	0.725	49h	1.925

1Ah	0.750	4Ah	1.950
1Bh	0.775	4Bh	1.975
1Ch	0.800	4Ch	2.000
1Dh	0.825	4Dh	2.025
1Eh	0.850	4Eh	2.050
1Fh	0.875	4Fh	2.075
20h	0.900	50h	2.100
21h	0.925	51h	2.125
22h	0.950	52h	2.150
23h	0.975	53h	2.175
24h	1.000	54h	2.200
25h	1.025	55h~7Fh	-
26h	1.050		
27h	1.075		
28h	1.100		
29h	1.125		
2Ah	1.150		
2Bh	1.175		
2Ch	1.200		
2Dh	1.225		
2Eh	1.250		
2Fh	1.275		

Note:

1. VCOMS is used for feed through voltage compensation.
2. Setting limitation: VCOMS = 0.1V~2.2V.

SSI_pos[8:0]: during “CMD 0x66 SSI” =1 .calculate based on panel X_resolution

SSI_pos = x_res/2 -1

‘-’: Don’t care

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	00h/00h/00h
S/W Reset	00h/00h/00h
H/W Reset	00h/00h/00h

VGH_VGL CTRL (BFh): VGH VGL Control

BFH	VGH_VGL CTRL (VGH_VGL Control)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VGH_VGL CTRL	0	↑	1	-	1	0	1	1	1	1	1	1	(BFh)
1st Parameter	1	↑	1	-	-	-	-	VGHP_DISP[4:0]					
2nd Parameter	1	↑	1	-	-	-	-	VGHP_TP[4:0]					
3rd Parameter	1	↑	1	-	-	-	-	VGHP_NOISE[4:0]					
4th Parameter	1	↑	1	-	-	-	-	-	VGLS_DISP[3:0]				
5th Parameter	1	↑	1	-	-	-	-	-	VGLS_TP[3:0]				
6th Parameter	1	↑	1	-	-	-	-	-	VGLS_NOISE[3:0]				

Description

VGHP_DISP/VGHP_TP/VGHP_NOISE[4:0]: VGH Set

VGHP[4:0]	VGH (V)	VGHP[4:0]	VGH (V)
00h	7.5	0Ch	13.5
01h	8.0	0Dh	14.0
02h	8.5	0Eh	14.5
03h	9.0	0Fh	15.0
04h	9.5	10h	15.5
05h	10.0	11h	16.0
06h	10.5	12h	16.5
07h	11.0	13h	17.0
08h	11.5	14h	17.5
09h	12.0	15h	18.0
0Ah	12.5	16h-1Fh	-
0Bh	13.0		

VGLS_DISP/VGLS_TP/VGLS_NOISE[3:0]: VGL Set

VGLS[3:0]	VGL (V)	VGLS[3:0]	VGH (V)
00h	6.46	08h	10.48
01h	7.02	09h	11.03
02h	7.51	0Ah	11.43

	03h	7.94	0Bh	12.07
	04h	8.54	0Ch	-
	05h	9.07	0Dh	-
	06h	9.51	0Eh	-
	07h	9.97	0Fh	-

Note:

1. VGHP - VGLS < 30v
2. VGHP_TP[4:0] / VGHP_NOISE[4:0] = VGHP_DISP[4:0] + 2v
3. Chip on Borad, VDDI=1.65 to 3.3V, VDD=2.65 to 3.3V, GND=0V,, Ta= -30℃~ 85℃

'-': Don't care

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h/00h/00h/00h/00h/00h
S/W Reset	00h/00h/00h/00h/00h/00h
H/W Reset	00h/00h/00h/00h/00h/00h

13.4 Command Table 3

COMMAND Table 3														
Instruction	**D/CX**	**WRX**	**RDX**	**PNUM**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
VCOMOFFSET	0	↑	1	2	1	1	1	0	0	0	1	1	(E3h)	VCOM_ OFFSET
	1	↑	1		0	VMF[6:0]								
	1	↑	1		-	VMF_NEW[6:0]								
GAMMA_ANA	0	↑	1		0	1	1	1	0	0	1	1	(73h)	Gamma_ Analog Setting
	1	↑	1		-	-	-	-	-	1	0	0		
	1	↑	1		GVDD_AD[3:0]				GVEE_AD[3:0]					
	1	↑	1		-	-	0	1	0	-	1	0		
	1	↑	1		-	VRP[6:0]								
	1	↑	1		-	VRN[6:0]								

VCOMOFFSET (E3h): VCOM OFFSET SET

E3H	VCMOFSET (VCOM OFFSET SET)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VCMOFSET	0	↑	1	-	1	1	0	1	1	1	0	1	(E3h)
1st Parameter	1	↑	1	-	0	VMF[6:0]							
2nd Parameter	1	↑	1	-	0	VMF_NEW[6:0]							

Description

VMF[6:0]/VMF_NEW[6:0]: finetune an offset to VCOM offset

VMF[6]	VMF[5:0]	VRP	VRN	VCOMS	VCOM
0	000000	VRP-64d	VRN+64d	VCM-64d	0
0	000001	VRP-63d	VRN+63d	VCM-63d	0
0	000010	VRP-62d	VRN+62d	VCM-62d	0
0	|	|	|	|	0
0	111110	VRP-2d	VRN+2d	VCM-2d	0
0	111111	VRP-1d	VRN+1d	VCM-1d	0
1	000000	VRP	VRN	VCM	0
1	000001	VRP+1d	VRN-1d	VCM+1d	0
1	000010	VRP+2d	VRN-2d	VCM+2d	0
1	|	|	|	|	0
1	111110	VRP+62d	VRN-62d	VCM+62d	0
1	111111	VRP+63d	VRN-63d	VCM+63d	0

'-': Don't care

Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	40h/40h
S/W Reset	40h/40h
H/W Reset	40h/40h

GAMMA_ANA (73h): Gamma Analog Setting

73H	GAMMA_ANA (Gamma Analog Setting)												
Inst / Para	D/CX	WRX	RDX	-	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMMA ANA	0	↑	1	-	0	1	1	1	0	0	1	1	(73h)
1st Parameter	1	↑	1	-	-	-	-	-	-	1	0	0	
2nd Parameter	1	↑	1	-	GVDD_AD[3:0]				GVEE_AD[3:0]				
3rd Parameter	1	↑	1	-	-	-	0	1	0	-	1	0	
4th Parameter	1	↑	1	-	-	VRP[6:0]							
5th Parameter	1	↑	1	-	-	VRN[6:0]							

Description

GVDD_AD[3:0]: positive gamma OP power set

GVDD_AD[3:0]	GVDD_AD (V)	GVDD_AD [3:0]	GVDD_AD (V)
00h	5.5	08h	6.3
01h	5.6	09h	6.4
02h	5.7	0Ah	6.5
03h	5.8	0Bh	6.6
04h	5.9	0Ch	6.7
05h	6.0	0Dh	6.8
06h	6.1	0Eh	-
07h	6.2	0Fh	-

GVEE_AD[3:0]: negative gamma OP power set

GVDD_AD[3:0]	GVDD_AD (V)	GVDD_AD [3:0]	GVDD_AD (V)
00h	3.4	08h	4.2
01h	3.5	09h	4.3
02h	3.6	0Ah	4.4
03h	3.7	0Bh	4.5
04h	3.8	0Ch	4.6
05h	3.9	0Dh	-
06h	4.0	0Eh	-
07h	4.1	0Fh	-

VRP[6:0]: VRP Set

VRP[6:0]	VRP (V)	VRP[6:0]	VRP (V)
00h	3.650 + (vcom offset)	40h	5.250 + (vcom offset)
01h	3.675 + (vcom offset)	41h	5.275 + (vcom offset)
02h	3.700 + (vcom offset)	42h	5.300 + (vcom offset)
03h	3.725 + (vcom offset)	43h	5.325 + (vcom offset)
04h	3.750 + (vcom offset)	44h	5.350 + (vcom offset)
05h	3.775 + (vcom offset)	45h	5.375 + (vcom offset)
06h	3.800 + (vcom offset)	46h	5.400 + (vcom offset)
07h	3.825 + (vcom offset)	47h	5.425 + (vcom offset)
08h	3.850 + (vcom offset)	48h	5.450 + (vcom offset)
09h	3.875 + (vcom offset)	49h	5.475 + (vcom offset)
0Ah	3.900 + (vcom offset)	4Ah	5.500 + (vcom offset)
0Bh	3.925 + (vcom offset)	4Bh	5.525 + (vcom offset)
0Ch	3.950 + (vcom offset)	4Ch	5.550 + (vcom offset)
0Dh	3.975 + (vcom offset)	4Dh	5.575 + (vcom offset)
0Eh	4.000 + (vcom offset)	4Eh	5.600 + (vcom offset)
0Fh	4.025 + (vcom offset)	4Fh	5.625 + (vcom offset)
10h	4.050 + (vcom offset)	50h	5.650 + (vcom offset)
11h	4.075 + (vcom offset)	51h	5.675 + (vcom offset)
12h	4.100 + (vcom offset)	52h	5.700 + (vcom offset)
13h	4.125 + (vcom offset)	53h	5.725 + (vcom offset)
14h	4.150 + (vcom offset)	54h	5.750 + (vcom offset)
15h	4.175 + (vcom offset)	55h	5.775 + (vcom offset)
16h	4.200 + (vcom offset)	56h	5.800 + (vcom offset)
17h	4.225 + (vcom offset)	57h	5.825 + (vcom offset)
18h	4.250 + (vcom offset)	58h	5.850 + (vcom offset)
19h	4.275 + (vcom offset)	59h	5.875 + (vcom offset)
1Ah	4.300 + (vcom offset)	5Ah	5.900 + (vcom offset)
1Bh	4.325 + (vcom offset)	5Bh	5.925 + (vcom offset)
1Ch	4.350 + (vcom offset)	5Ch	5.950 + (vcom offset)
1Dh	4.375 + (vcom offset)	5Dh	5.975 + (vcom offset)
1Eh	4.400 + (vcom offset)	5Eh	6.000 + (vcom offset)
1Fh	4.425 + (vcom offset)	5Fh	6.025 + (vcom offset)
20h	4.450 + (vcom offset)	60h	6.050 + (vcom offset)
21h	4.475 + (vcom offset)	61h	6.075 + (vcom offset)

22h	4.500 + (vcom offset)	62h	6.100 + (vcom offset)
23h	4.525 + (vcom offset)	63h	6.125 + (vcom offset)
24h	4.550 + (vcom offset)	64h	6.150 + (vcom offset)
25h	4.575 + (vcom offset)	65h	6.175 + (vcom offset)
26h	4.600 + (vcom offset)	66h	6.200 + (vcom offset)
27h	4.625 + (vcom offset)	67h	6.225 + (vcom offset)
28h	4.650 + (vcom offset)	68h	6.250 + (vcom offset)
29h	4.675 + (vcom offset)	69h	6.275 + (vcom offset)
2Ah	4.700 + (vcom offset)	6Ah	6.300 + (vcom offset)
2Bh	4.725 + (vcom offset)	6Bh	6.325 + (vcom offset)
2Ch	4.750 + (vcom offset)	6Ch	6.350 + (vcom offset)
2Dh	4.775 + (vcom offset)	6Dh	6.375 + (vcom offset)
2Eh	4.800 + (vcom offset)	6Eh	6.400 + (vcom offset)
2Fh	4.825 + (vcom offset)	6Fh	6.425 + (vcom offset)
30h	4.850 + (vcom offset)	70h	6.450 + (vcom offset)
31h	4.875 + (vcom offset)	71h	6.475 + (vcom offset)
32h	4.900 + (vcom offset)	72h	6.500 + (vcom offset)
33h	4.925 + (vcom offset)	73h	6.525 + (vcom offset)
34h	4.950 + (vcom offset)	74h	6.550 + (vcom offset)
35h	4.975 + (vcom offset)	75h	6.575 + (vcom offset)
36h	5.000 + (vcom offset)	76h	6.600 + (vcom offset)
37h	5.025 + (vcom offset)	77h	6.625 + (vcom offset)
38h	5.050 + (vcom offset)	78h	6.650 + (vcom offset)
39h	5.075 + (vcom offset)	79h	6.675 + (vcom offset)
3Ah	5.100 + (vcom offset)	7Ah	6.700 + (vcom offset)
3Bh	5.125 + (vcom offset)	7Bh	6.725 + (vcom offset)
3Ch	5.150 + (vcom offset)	7Ch	6.750 + (vcom offset)
3Dh	5.175 + (vcom offset)	7Dh	6.775 + (vcom offset)
3Eh	5.200 + (vcom offset)	7Eh	6.800 + (vcom offset)
3Fh	5.225 + (vcom offset)	7Fh	6.825 + (vcom offset)

VRN[6:0]: VRN Set

VRN[6:0]	VRN (V)	VRN[6:0]	VRN (V)
00h	-1.875 + (vcom offset)	40h	-3.475 + (vcom offset)
01h	-1.9 + (vcom offset)	41h	-3.5 + (vcom offset)

02h	-1.925 + (vcom offset)	42h	-3.525 + (vcom offset)
03h	-1.95 + (vcom offset)	43h	-3.55 + (vcom offset)
04h	-1.975 + (vcom offset)	44h	-3.575 + (vcom offset)
05h	-2 + (vcom offset)	45h	-3.6 + (vcom offset)
06h	-2.025 + (vcom offset)	46h	-3.625 + (vcom offset)
07h	-2.05 + (vcom offset)	47h	-3.65 + (vcom offset)
08h	-2.075 + (vcom offset)	48h	-3.675 + (vcom offset)
09h	-2.1 + (vcom offset)	49h	-3.7 + (vcom offset)
0Ah	-2.125 + (vcom offset)	4Ah	-3.725 + (vcom offset)
0Bh	-2.15 + (vcom offset)	4Bh	-3.75 + (vcom offset)
0Ch	-2.175 + (vcom offset)	4Ch	-3.775 + (vcom offset)
0Dh	-2.2 + (vcom offset)	4Dh	-3.8 + (vcom offset)
0Eh	-2.225 + (vcom offset)	4Eh	-3.825 + (vcom offset)
0Fh	-2.25 + (vcom offset)	4Fh	-3.85 + (vcom offset)
10h	-2.275 + (vcom offset)	50h	-3.875 + (vcom offset)
11h	-2.3 + (vcom offset)	51h	-3.9 + (vcom offset)
12h	-2.325 + (vcom offset)	52h	-3.925 + (vcom offset)
13h	-2.35 + (vcom offset)	53h	-3.95 + (vcom offset)
14h	-2.375 + (vcom offset)	54h	-3.975 + (vcom offset)
15h	-2.4 + (vcom offset)	55h	-4 + (vcom offset)
16h	-2.425 + (vcom offset)	56h	-4.025 + (vcom offset)
17h	-2.45 + (vcom offset)	57h	-4.05 + (vcom offset)
18h	-2.475 + (vcom offset)	58h	-4.075 + (vcom offset)
19h	-2.5 + (vcom offset)	59h	-4.1 + (vcom offset)
1Ah	-2.525 + (vcom offset)	5Ah	-4.125 + (vcom offset)
1Bh	-2.55 + (vcom offset)	5Bh	-4.15 + (vcom offset)
1Ch	-2.575 + (vcom offset)	5Ch	-4.175 + (vcom offset)
1Dh	-2.6 + (vcom offset)	5Dh	-4.2 + (vcom offset)
1Eh	-2.625 + (vcom offset)	5Eh	-4.225 + (vcom offset)
1Fh	-2.65 + (vcom offset)	5Fh	-4.25 + (vcom offset)
20h	-2.675 + (vcom offset)	60h	-4.275 + (vcom offset)
21h	-2.7 + (vcom offset)	61h	-4.3 + (vcom offset)
22h	-2.725 + (vcom offset)	62h	-4.325 + (vcom offset)
23h	-2.75 + (vcom offset)	63h	-4.35 + (vcom offset)
24h	-2.775 + (vcom offset)	64h	-4.375 + (vcom offset)
25h	-2.8 + (vcom offset)	65h	-4.4 + (vcom offset)
26h	-2.825 + (vcom offset)	66h	-4.425 + (vcom offset)

27h	-2.85 + (vcom offset)	67h	-4.45 + (vcom offset)
28h	-2.875 + (vcom offset)	68h	-4.475 + (vcom offset)
29h	-2.9 + (vcom offset)	69h	-4.5 + (vcom offset)
2Ah	-2.925 + (vcom offset)	6Ah	-4.525 + (vcom offset)
2Bh	-2.95 + (vcom offset)	6Bh	-4.55 + (vcom offset)
2Ch	-2.975 + (vcom offset)	6Ch	-4.575 + (vcom offset)
2Dh	-3 + (vcom offset)	6Dh	-4.6 + (vcom offset)
2Eh	-3.025 + (vcom offset)	6Eh	-4.625 + (vcom offset)
2Fh	-3.05 + (vcom offset)	6Fh	-4.65 + (vcom offset)
30h	-3.075 + (vcom offset)	70h	-4.675 + (vcom offset)
31h	-3.1 + (vcom offset)	71h	-4.7 + (vcom offset)
32h	-3.125 + (vcom offset)	72h	-4.725 + (vcom offset)
33h	-3.15 + (vcom offset)	73h	-4.75 + (vcom offset)
34h	-3.175 + (vcom offset)	74h	-4.775 + (vcom offset)
35h	-3.2 + (vcom offset)	75h	-4.8 + (vcom offset)
36h	-3.225 + (vcom offset)	76h	-
37h	-3.25 + (vcom offset)	77h	-
38h	-3.275 + (vcom offset)	78h	-
39h	-3.3 + (vcom offset)	79h	-
3Ah	-3.325 + (vcom offset)	7Ah	-
3Bh	-3.35 + (vcom offset)	7Bh	-
3Ch	-3.375 + (vcom offset)	7Ch	-
3Dh	-3.4 + (vcom offset)	7Dh	-
3Eh	-3.425 + (vcom offset)	7Eh	-
3Fh	-3.45 + (vcom offset)	7Fh	-

'-': Don't care

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	04h/88h/1Ah/66h/4Dh
S/W Reset	04h/88h/1Ah/66h/4Dh
H/W Reset	04h/88h/1Ah/66h/4Dh

14 REVISION HISTORY

Version	Date	Description
V0.0	2022/02	Preliminary
V0.1	2023/06	Modify CMD Table Add Touch Application